Tracking Phase Noise In Short-Range Radios

Part 4 of this series on short-range radio will show how the signal source design plays an important role in the ultimate performance of a short-range radio sys-

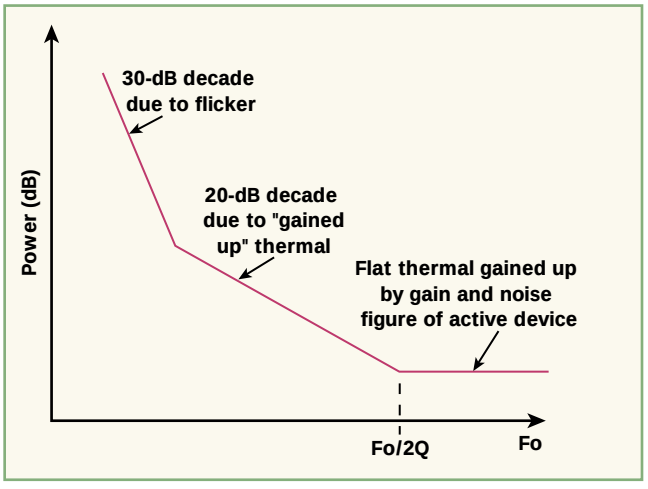
Oscillator phase noise is often associated with receiver (Rx) sensitivity analyses. But in the design of a short-range radio system, especially those employing integrated low Q voltage-controlled-oscillator (VCO) methods, excessive phase noise can limit the effectiveness of a modulation scheme to transmit information. Too much phase noise can raise the effective bit-error rate (BER) of the system and prevent transmitted information from being accurately received.

Oscillator phase noise may be intuitively defined as the noise attached to and spread around the carrier that is measured in the frequency domain. In this sense, it is similar to intended modulation and, if bad enough, interferes with desired modulation. It is generally measured on a per Hertz of frequency basis at some offset from the carrier and expressed in decibels relative to the total carrier power. Examination of the most important phase-noise issues of low-power VCOs is as follows. The induced sideband-to-carrier ratio, a peak-voltage magnitude-based ratio, is developed from small-signal frequency-modulation (FM) theory and is provided by:

[SEE EQ. 31 BELOW]

where:

$$(Sideband\ mag/Carrier\ mag)(f) = \left[V_p(f)K_0\right]/2f \qquad (31)$$



6. This plot shows basic VCO phase-noise characteristics.

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$V_p(f)$ = the peak value of a sinusoidal baseband modulating voltage at frequency f on the steering input to the VCO and:

K_Θ = the gain of the VCO (in Hz/V.

The induced sidebands occur on both sides of the carrier. This equation is typically used to predict discrete spurs such as synthesizer sidebands (using Fourier series to obtain sinusoids), but it is also useful for broadband noise sources. A small transformation is needed to apply to these sources. Since $V_p(f)$ is a peak value and noise sources would typically be expressed in root mean square (RMS), it is possible to write the sideband to carrier power ratio based on RMS noise voltage, $V_n(f)$, as:

[SEE EQ. 32 BELOW]

The sideband-to-carrier power ratio of Eq. 32 is the contribution of tuning input noise to the general phase noise L(f) that will be defined shortly. Taking 10log[S/C] will provide the contribution to phase noise from this source in units of decibels above the carrier per Hertz. An example of the effect of Eq. 32 is the phase-noise effect of the flicker noise of an operational amplifier that is used in a loop filter or buffer driving a VCO. This seldom-mentioned unpleasant fact is actually one of the primary reasons behind the modern prevalence of the current-pump PLL. The current pump is off more than 99 percent of the time, greatly reducing its flicker noise and often leaving the dominant noise source in the VCO input as the resistor in the passive loop filter. The phase-noise contribution from large resistors in series with the tune line, or the resistor in the loop filter, can also be calculated from Eq. 32. Another place it comes in extremely handy is the induced phase noise from power supply and ground. Even when the power

$$(Sideband\ pwr/Carrier\ pwr)\,(f) = \left\{\left[V_n(f)K_0\right] / \left(\sqrt{2}f\right)\right\}^2 \quad (32)$$

Table 6: Integrated PLL transmitter phase-noise-limited signal-to-noise ratio

FLICKER CORNER (kHz)	LOOP NAT. FREQ. (kHz)	VCO LOADED Q	PHASE-NOISE-LIMITED SNR (dB)	COMMENT
1	10	1	6.5	BiCMOS process, relaxation (no resonator) VCO
	20	1	14.9	
	30	1	20.7	Minimum acceptable SNR = 20 dB
	50	1	28.5	
	100	1	37.7	
1	2	4	7.7	BiCMOS process, LC VCO with integrated inductor
	4	4	11.0	
	10	4	18.4	
	15	4	23	Need 12 kHz for 20 dB
	30	4	32	
1	1	10	13.1	BiCMOS process, LC VCO with heavily loaded external chip inductor
	4	10	18.3	
	10	10	25.6	Need 5.4 kHz for 20 dB
1	0.5	30	18.2	BiCMOS process, LC VCO with lightly loaded external air-core inductor
	2	30	20.9	Need 1.5 kHz for 20 dB
	10	30	31.0	
100	50	1	17.7	CMOS process, relaxation (no resonator) VCO
	100	1	26.1	Need 64 kHz for 20 dB
100	20	4	12.7	CMOS process, LC VCO with integrated inductor
	50	4	23.1	Need 41 kHz for 20 dB
100	10	10	11.8	CMOS process, LC VCO with external chip inductor
	20	10	19.3	
	25	10	21.4	Need 23 kHz for 20 dB
100	10	30	18.5	CMOS process, LC VCO with external air-core inductor
	20	30	23.3	

supply is linearly regulated and supposedly quiet, it has flicker noise that can dominate the phase-noise profile. To calculate this noise, one uses Eq. 32 where K_θ becomes $K_{\theta p}$, the frequency change per volt of power-supply change. This term is usually only a decade or so down from K_θ, and can easily dominate. Many a designer has done a good job on the standard phase-noise control issues and has then been unpleasantly surprised by a power-noise-dominated phase noise up to several tens of decibels worse than predicted.

The oscillator design itself is inherently phase noisy even when the tune and power lines are sufficiently quiet. A relatively accurate expression for oscillator phase noise (derived from forms provided in refs. 6 and 7) from factors within the oscillator is given by Eq. 33:

[SEE EQ. 33 BELOW]

where:

S_ϕ = the double-sided spectral density of phase fluctuation (in rad^2/Hz),

f_0 = oscillator carrier or operating frequency,

f = the offset frequency from the carrier at which phase noise is measured in a 1-Hz bandwidth,

f_c = the flicker-noise corner frequency of the oscillator active device, the frequency where flicker noise (1/f noise) on the output of the device is equal to the thermal floor multiplied by gain and noise factor,

Q = loaded Q of the resonator,

G = oscillator active-device gain in compression,

F = oscillator active-device noise factor (not in decibels) in compression, typically higher than the uncompressed noise factor,

kT = Boltzman s constant and absolute temperature, and

P_0 = the output power of the oscillator s active device.

The term S_ϕ shall be momentarily related to what is commonly referred to as phase noise. This equation is basically Leeson s phase-noise model with a flicker-noise corner added, and with power on the output side of the amplifier to more clearly show

$$S_\phi(f) = \left[(f_o/2Q)^2(GFkT/P_0)f_c/f^3\right] + \left[(f_o/2Q)^2(GFkT/P_0)/f^2\right] + \left[(GFkT/P_0)f_c/f\right] + \left[(GFkT/P_0)\right] \quad (33)$$

$$L(f) = \left[(f_o/2Q)^2 (GFkT/2P_0) f_c/f^3\right] + \left\{(f_o/2Q)^2 (GFkT/2P_0) + \left[(V_{n1}(f)K_0)/\sqrt{2}\right]^2 + \left[(V_{n2}(f)K_{0p})/\sqrt{2}\right]^2\right\}/\left[f^2\right] + \left[(GFkT/2P_0) f_c/f\right] + (GFkT/2P_0) \quad (36)$$

the effect of active-device gain G.

The somewhat nonintuitive term spectral density of phase fluctuation may be, using a small angle approximation, interpreted as the noise spectral-density ratio relative to carrier power commonly known as phase noise. Phase noise is sometimes provided as $L(F_0) = 10\log(S_\phi/2)$ in units of decibels above the carrier per Hertz. Since linear and decibel units can be considered here, it might be wise to make more clear definitions:

$$L(f) = S_\phi(f)/2 \quad (34)$$

$$L(dB)(f) = 10\log\left[S_\phi(f)/2\right] \quad (35)$$

The factor of 1/2 comes from the convention that phase noise as a power-spectral density is real and observed on one side, while the phase-fluctuation spectral density has double the power in that it represents the phase fluctuation in a 1-Hz bandwidth on both sides of the carrier.

A typical VCO free-running phase noise shape is shown in Fig. 6, where it will be noted there are only three main regions despite the fact that Eq. 33 has four terms. The 1/f term has been left out since the $1/f^2$ term dominates it in most cases. For bipolar transistors, the flicker corner can be from below 100 Hz to several kilohertz. For complementary metal-oxide semiconductor (CMOS), the flicker corner is typically from several tens of kilohertz to 1 MHz or slightly more. The $1/f^2$ rise in phase noise begins at the resonator half-bandwidth, or $f_0/2Q$. For the typical Q values and center frequencies of RF oscillators, this is well-beyond the 1/f corner, so the term 1/f never catches up. However, for low-frequency, high-Q oscillators such as crystal oscillators, the 1/f term can be noticed, particularly for CMOS with its high flicker noise.

Equation 33 may be extended to include the effects of the tuning and power-supply noise by adding the appropriate forms of Eq. 32 to Eq.

33. This is a requirement for the high-gain VCOs typical of integrated short-range radios. Doing this and converting to phase noise in watts (noise) per watt (carrier) per Hertz through Eq. 34 yields

Eq. 36:

[SEE EQ. 36 ABOVE]

where:

V_{n1} = RMS spectral-noise density on the tune line,

V_{n2} = RMS spectral-noise density on the power line,

K_0 = VCO gain (in Hz/V), and

K_{0p} = the power-supply-pulling susceptibility of the VCO (in Hz/V).

This equation allows quick visualization of the design methods used to minimize oscillator phase-noise noise. These are to maximize loaded Q, maximize output power (simultaneous voltage and current compression in the active device will extract the most power from the available budget), minimize flicker factor (bipolar is superior to FETs), minimize loop gain (3 to 6 dB over loop losses), minimize compressed noise figure (minimum compression helps for this), minimize VCO gain and input noise, and minimize pulling frequency susceptibility and noise on the supply.

Parameter V_{n1} is primarily resistive thermal noise and active device flicker noise. If an opamp drives a VCO input, its flicker noise is likely to dominate the phase noise, especially for low-power CMOS opamps. For current-pump-based PLLs, the flicker noise will be low since the pulse width of the current pumps will approach zero (unless the VCO is directly FSK modulated, when the phase detector will encode this modulation when the loop attempts to hold the VCO exactly on frequency). Thus, for current-pump PLLs, V_{n1} may be primarily thermal noise. Given the typically small current pump values, and typically wide loop bandwidth in short-range radios, this resistor is typically much larger than that used in the loop filter of a design such as a cellular-telephone synthesizer. With the high VCO gain typical of short-range radios, its thermal noise is often quite noticeable. It is calculated using the standard equation:

$$V_n(rms) = (4kTR)^{0.5} \qquad (37)$$

The common practice of following a second-order loop filter (two capacitors, one resistor, which makes a third-order loop) with a second RC stage (resulting in a fourth-order loop) must be viewed with caution in short-range radios. To avoid loading the loop filter with this last stage, this second resistor is normally made 5 to 10 times larger than the damping resistor and thus it has that much more thermal noise. Equations 36 and 37 in concert with the closed-loop phase-noise analysis described below should be used to check if this additional resistor and even the standard loop resistor are acceptable.

Phase-Noise Analysis

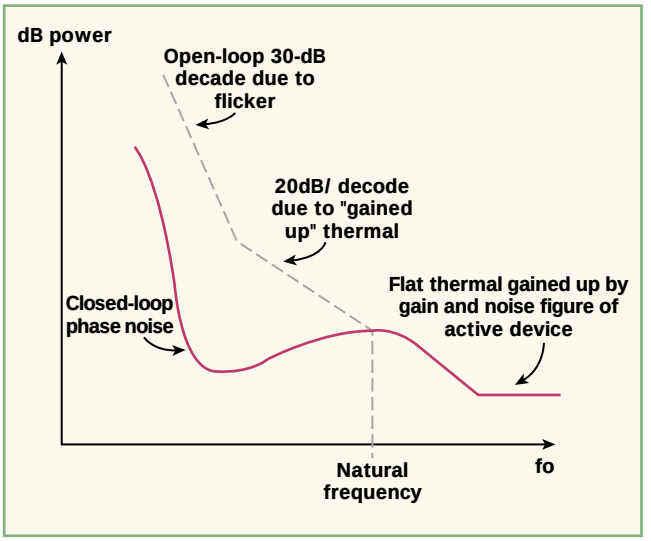
The earlier statement that the wideband PLL could cover noise problems in the VCO will now be proved and analyzed. From Eq. 32 it is clear that phase noise may be referred to the input as a noise voltage in a way analogous to how noise in amplifiers can be referred to their input. If the oscillator is imagined as noiseless and all phase noise is induced by an imaginary RMS VCO open-loop noise voltage, V_{nvo}, on the VCO tune input, and noting that total sideband to carrier power ratio is the same as L(f), then Eq. 32 may be solved for V_{nvo} as:

$$V_{nvo} = \left\{ f\left[2L(f)\right]^{0.5}/K_0 \right\} \quad (38)$$

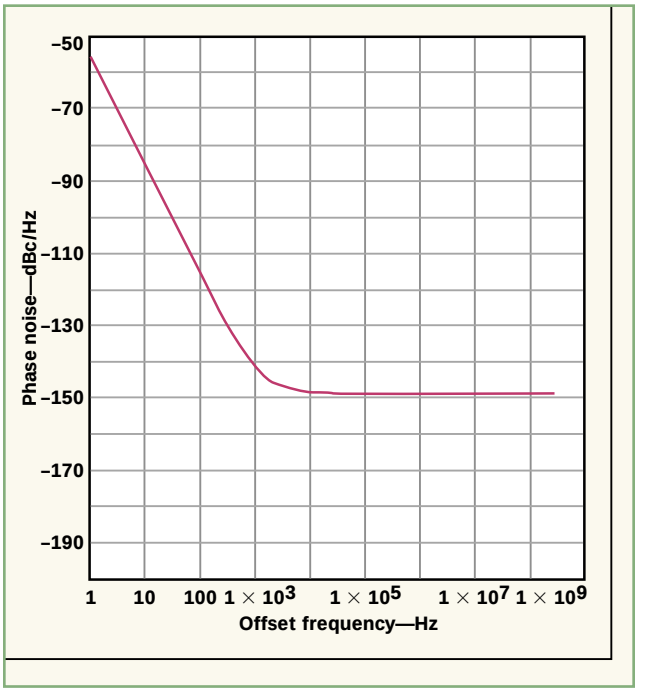
This is the input-referenced open-loop VCO noise, where L(f) is given by Eq. 36. However, the open-loop input-referenced noise will be modified by the closed-loop action of the PLL. The PLL will reduce the noise within the loop bandwidth in the attempt to keep the phase error equal to zero. It may be shown by basic analysis of Fig. 4 (in Part 3) that the effect of the loop on the open-loop input-referenced VCO phase noise is exactly equal to multiplying by the magnitude of He(s). That is, the injected noise V_{nvo} that models free-running phase noise is modified by the loop to be the RMS closed-loop noise voltage quantity V_{nvc} residing directly on the tune voltage, and this voltage is found by:

$$V_{nvc} = V_{nvo}\left|H_e(s)\right| \quad (39)$$

This function can be used in the standard second-order normal-



7. This plot shows typical wideband PLL VCO phase noise. The integral of the area between the open- and closed-loop phase noise is the noise power removed by the loop filter.



8. This plot is an example of the phase noise for a crystal oscillator.

ized form given earlier, or for high accuracy in higher-order loops, it can be calculated based on the full set of intended and parasitic poles in the loop.

Next, the question of crystal-oscillator phase noise and its effect will be addressed. Although a crystal oscillator exhibits high Q and inherently low phase noise, its phase noise is much worse in CMOS high flicker processes, and is it then multiplied by divider value N through the closed-loop action of the PLL. While the crystal reference for a cellular telephone is typically a well-optimized bipolar device consuming about 2 mA, the crystal oscillator for a short-range transmitter typically consumes 200 µA and is often implemented with a CMOS digital gate active device that has typically higher noise figure and much higher flicker noise than a bipolar transistor. Referring to Eq. 36, the increase in phase noise for this short-range reference (compared to a cellular-telephone reference) would typically be on the order of 20 to 40 dB. This combination of factors is such that effect of the phase noise of the crystal oscillator on the total closed-loop phase noise is definitely not negligible for short-range FSK systems.

Analysis of the transfer functions of the closed-loop PLL will show that:

$$V_{nxc} = V_{nx}\left(K_{ox}N/MK_0\right)\left|H(s)\right| \quad (40)$$

where:

V_{nxc} = the closed-loop RMS noise that appears on the VCO input (not the VCXO input) as a result of crystal-oscillator phase noise,

V_{nx} = crystal-oscillator noise referred to the crystal-oscillator steering input (a VCXO),

K_{ox} = the crystal-oscillator tune slope (in Hz/V),

M = the value of any divider between the crystal oscillator and the phase detector, and

H(s) = the phase-transfer function.

The method of representing crystal- oscillator phase noise as referred to a tune input is useful because many references are VCXOs to allow exact frequency trim, which is then susceptible to noise on the tune line from thermal, flicker, and power-supply noise sources that should be taken into account. The effect of supply noise on the crystal oscillator is taken into account just as it was for the VCO, though K_0 and K_{0p} for the crystal will be much lower than the corresponding tune slopes for the VCO. If the crystal oscillator is not a VCXO, then an arbitrary value for K_{ox} can be assumed for the purpose of this calculation.

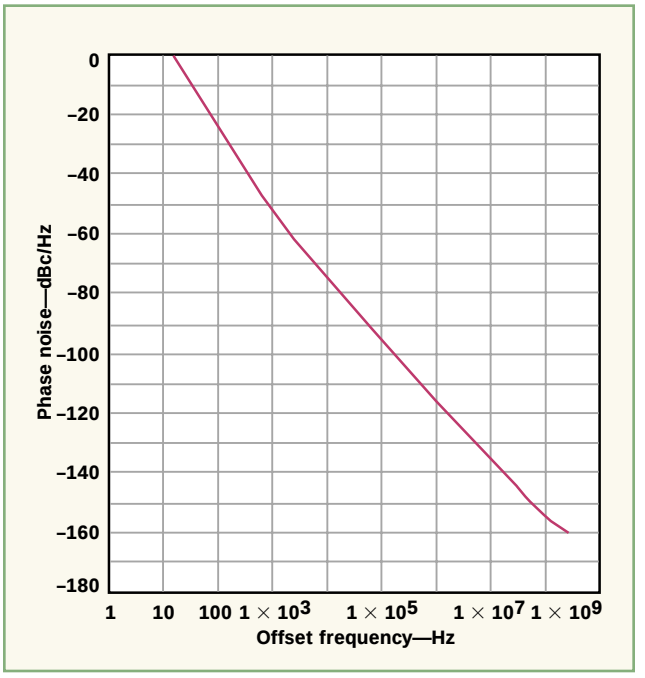
The total noise from the VCO, V_{ntc}, and the crystal oscillator referred to the input of the VCO from these rms referred to VCO input voltages in the closed-loop state is:

$$V_{ntc} = \left(V_{nvc}^2 + V_{nxc}^2\right)^{0.5} \quad (41)$$

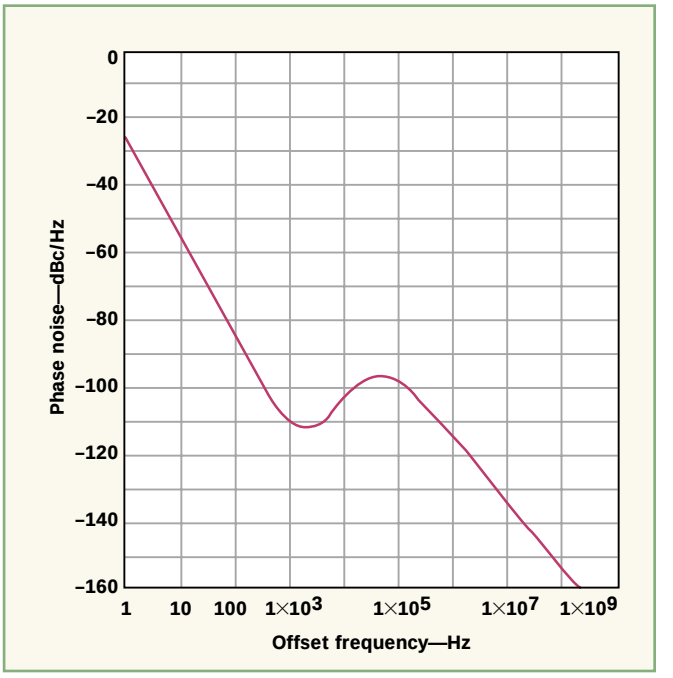
To get the total resulting closed-loop phase noise, V_{ntc} is then applied back through Eq. 32 to get

$$Lc(f) = \left\{\left[V_{ntc}(f)K_0\right]/\sqrt{2}f\right\}^2 \quad (42)$$

The effect of the closed loop on PLL noise is especially dramatic for a wideband loop (Fig. 7). Well inside the loop s natural frequency, the noise is suppressed 40 dB



9. This plot is an example of the phase noise for a free-running



10. This plot shows an example of a short-range transmitter s

per decade (a second-order magnitude transfer function). If the loop natural frequency is out where the VCO phase noise is at 20 dB per decade, and other noise sources do not limit loop action, then the phase noise will decline 20 dB per decade over that frequency segment. A common occurrence is for divider noise (not shown in this model) to limit this effect, typically so that the phase noise approximately flattens out at some offset well inside the loop bandwidth. Also, the loop can only reduce noise to the point of the multiplied crystal reference noise as given by Eq. 40, which is why the phase noise turns around and starts rising again. However, crystal oscillators have very low phase noise due to their very high Q, and so despite degradations such as divider noise a wideband PLL can provide a high degree of phase-noise clean up. It is this action that allows low Q integrated VCOs such as relaxation oscillators, usually running on unregulated supplies, to provide adequate performance for FSK modulation.

As an example, the model presented above has been implemented as a MathCAD model to analyze the performance of a typical BiCMOS transmitter implementation. The following basic parameters apply. The crystal oscillator has a frequency of 13.5625 MHz, a loaded Q of 5000, a flicker corner frequency of 1 kHz, an active device noise factor of 10, gain of 6 dB, current consumption of 250 μA, Z_{out} of 2000 Ω, and output power of 63 μW. The VCO has a frequency of 434 MHz, a Q of 1 (a relaxation oscillator), a flicker corner frequency of 1 kHz, an active device noise factor of 10, compressed gain of 6 dB, current consumption of 3 mA, output impedance of 300 Ω, output power of 1.35 mW, and K_0 = 200 MHz/V. The PLL has a natural frequency of 50 kHz, a damping factor of 1.2, current-pump current of 260 μA, N = 32, M = 1, filter R = 470 Ω, and filter C = 0.015 μF.

The resulting phase noise of the crystal oscillator, the open-loop VCO, and the closed-loop PLL are shown in Figs. 8, 9, and 10. For the crystal oscillator with its very high Q, the $1/f^3$ term is the first to rise above the floor. The VCO phase-noise curve rising above 0 dB at very low offset frequency is not what actually happens, as physically L(dB)(f) must flatten at 0 dB. This error is due to the 1-Hz granularity assumed in the phase noise not being adequate as the offset approaches 1 Hz, which is particularly apparent in this low-Q, high-flicker-noise case. The closed-loop noise model shows the effect of the 50-kHz-wide loop on the poor phase noise of the relaxation VCO. It may be noted that the phase noise at offsets lower than 1 kHz is equal to the crystal-oscillator phase noise plus $10\log N^2$ dB, as would be expected from the PLL multiplying the reference by N (here N = 32). This phase noise will limit demodulated FSK signal-to-noise

$$(S/N)[\text{phase noise bounded}] = 10\log\left(f_{rms}^2/\Delta f^2\right) \qquad (44)$$

ratio (SNR) to approximately 28 dB no matter how strong the receiver input SNR.

Short-range radio systems are almost totally ASK or FSK modulation, since these modes are the lowest power and simplest to implement. For ASK systems phase noise is not a serious issue unless it is so bad that it places noticeable energy outside the receive bandwidth or fails regulatory requirements (see Part 2 of this article series, October 2001, p. 79). But for digital FSK (becoming especially popular in Europe) the phase-noise sets an upper limit on the signal-to-noise ratio that may be achieved. It is desired for this limit to be high enough that in practice it is not a noticeable factor in BER, which generally calls for the this limit to be 20 dB or more.

If a phase noisy unmodulated carrier is detected with a sensitive FM demodulator, the output will display a noise referred to as the residual frequency modulation, which is a noise that competes with the desired FSK. For integrated phase noise less than 1 rad^2, the square of RMS residual FM due to phase noise over the bandwidth f_a to f_b is given by (ref. 7):

$$\Delta f^2 = 2\int_{f_a}^{f_b} f^2 L(f)df \qquad (43)$$

This noise sets a limit on FSK SNR for intended FSK expressed as one-sided RMS frequency deviation f_{rms} that is given by:

[SEE EQ. 44 BELOW]

The limits of integration selected in Eq. 43 depend on the data rate and protocol used in the system, and the acceptable BER. The cascade of baseband filtering in the transmitter and receiver generally sets these limits. Sometimes this filtering may be pure lowpass and extend all the way to DC, but it is common for something in the system or circuit design to force a low-frequency highpass function such that the baseband filtering is actually bandpass. For example, FSK PLL modulation imposed by direct modulation of the VCO with correcting integrator to reduce distortion (see US patent No. 6172579) cannot modulate all the way to DC. The rfPIC12C509 with FSK via the crystal reference does go all the way to DC, but the receiver may not necessarily go all the way to DC. For example, the Rx demodulator may be highpass filtered to remove DC offsets. Rx automatic frequency control (AFC) also sets a lower limit on the frequency content of the demodulated FSK output, the effect of which is to place one or more highpass poles at the AFC system bandwidth. If any of these highpass poles are present, they suppress phase noise below the poles and provide a good number to use for f_a in Eq. 43. However, if the protocol used has noticeable low frequency content, then AC coupling in the system above this content will degrade BER by removing desired energy. For example, at 20 kb/s using a non-return-to-zero (NRZ) protocol an AC-coupled highpass response will degrade BER the equivalent of only about 1/10 of a dB of SNR for a 10-Hz corner frequency, but at 50 Hz will degrade BER by about 1-dB equivalent reduction in SNR. A Manchester format with zero DC content would have less susceptibility to highpass coupling in the system. A rule of thumb for selecting f_a for DC-coupled systems is to set it a 0.1 percent for NRZ and 1 percent for Manchester, for which accuracy should be to within a small fraction of 1 dB. For the upper limit of integration f_b, select the lowest pole of the baseband lowpass filtering, typically about one-half the data rate for binary FSK.

The phase-noise-limited FSK signal to noise ratio may now be examined, with highly enlightening results for the design of integrated short-range transmitters. Incorporating Eqs. 43 and 44 into a MathCad model allows running up a variety of cases of process flicker noise, VCO Q, and the PLL parameters. The final result of this is to give the necessary PLL bandwidth to provide a minimum acceptable SNR. The case examined is a data rate of 20 kb/s, NRZ formatted, with a frequency deviation of 20 kHz peak-to-peak (modulation index = peak-to-peak deviation/data rate = 1.0), with lowpass filtering at 10 kHz (bandwidth-time product BT = 0.5). The limits of phase-noise integration for this case are chosen as 10 Hz and 10 kHz. The phase-noise cases will range from a BiCMOS process with flicker corner of 1 kHz to a CMOS process with flicker corner of 100 kHz, with VCO Qs ranging from 1 (relaxation oscillator) to 30 (LC with off-die air-core inductor), and with loop natural frequency ranging from 500 Hz to 100 kHz.

Many interpretations can be made from the results of Table 6. Interpolating Table 6 for a 20-dB SNR for the hypothetical BiCMOS process, relaxation oscillators require a loop natural frequency of 30 kHz or more, integrated inductor LC VCOs require a loop natural frequency of about 12 kHz or more, external chip-inductor-based LC VCOs require about 5.4 kHz or more, and external air-core-inductor-based VCOs require a loop natural frequency of about 1.5 kHz or more. For the hypothetical CMOS process, relaxation oscillators require a loop natural frequency of approximately 64 kHz or more, devices with on-chip inductors around 41 kHz, with chip inductors about 23