Microwaves&RF

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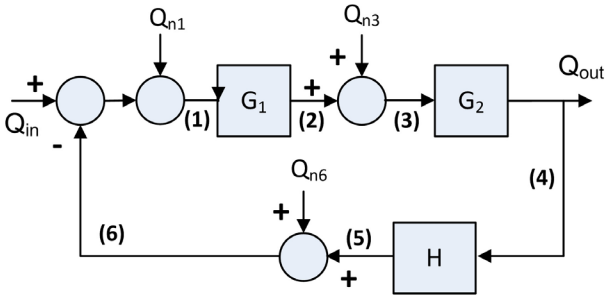
Noise and its Shaping in Ultra-Low Noise Synthesizer Design

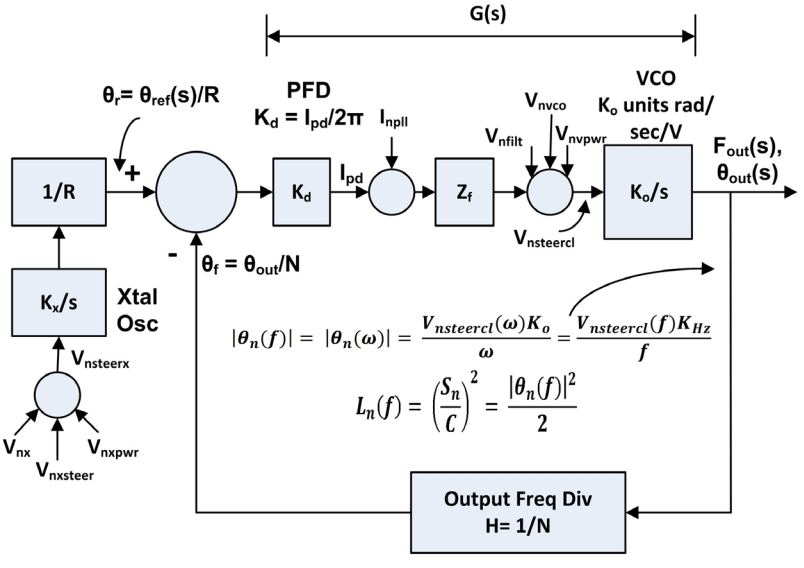
The third installment in a five-part series, this article dives into topics like noise transfer functions and total synthesizer noise.

This third part in our low-noise synthesizer design series is the medium-length online version. In print are the abridged versions, while full-length versions are available at www.longwingtech.com. Part 1 (Dec. 2018) covered basic design for functionality and stability. Part 2 (Feb. 2019) covered the many noise sources in the synthesizer outside of the actual synthesizer IC. This third article looks into synthesizer IC noise, the closed-loop shaping of noises, and related issues such as optimum bandwidth.

Here, a key metric for characterizing synthesizer IC noise is developed. This material also leads directly to analysis of optimum loop bandwidth, taking all noise sources into account—a key design topic that to the author's knowledge is not published elsewhere. For reasons of space, some important parts of this subject are deferred to the full version on the Longwing website. The long-version material includes derivation of charge-pump noise in current form, spur noise, SPICE modeling of PLL noise, and application noise requirements. Part 4 will review parts and tools available to the low-noise synthesizer designer. The concluding Part 5



1. A generalized feedback tracking loop with noise "Q" injected at various spots is useful for deriving the noise transfer functions from a point "y" to a point "z." Here, the forward gain G is broken up into G_1 and G_2 for generality.



2. General PLL block diagram with noise sources. Note the phase noise equations contained in the figure for converting rms summed voltage noise Vnsteer to phase noise, which were derived earlier. Many noise sources use a math processing program like Mathcad or MatLab, which is recommended for calculations and graphs of noise terms and total noise. SPICE may also be used to build a behavioral model of the loop that provides noise.

will present low-noise design examples.

Recent years have seen major changes in the frequency synthesis art. Ultra-low-noise discrete VCOs, which still enjoy a 20- to 30-dB phase-noise superiority over the best integrated VCOs, are no longer always the preferred solution. Integrated VCOs are now paired with sigma-delta fractional-N architectural innovations, often allowing them to have not only surprisingly good noise performance, but often superior performance, particularly for applications where closer in phase noise is the issue.

The ways to achieve such performance may be understood from the noise-shaping material in this article. The ultra-low-noise discrete VCO remains superior for higher offset frequency (beyond the loop bandwidth). Part 5 will provide an example illustrating how discrete VCO design could potentially be extended to use these same methods to maintain superior performance at lower offsets. It remains to be seen whether such designs allowing discrete VCOs to recapture their originally superior noise performance in the locked state will emerge.

Noise Transfer Functions and Total Synthesizer Noise

Part 2 gave the main open-loop noise sources in the PLL. Now, we turn our attention to how these noises are shaped *by* the PLL into the closed-loop noise. A fundamental feature of the modern, high bandwidth PLL is that the very low noise of the input crystal reference is transferred to the VCO, for frequencies within the loop bandwidth, down to the noise floor allowed by the synthesizer IC's own noise (dividers and charge pump). Beyond the loop bandwidth, the VCO reverts to its own free-running noise, hopefully only slightly degraded by filter and power-supply noise.

In Part 1 of this series, particularly the online and full versions, the transfer functions pertinent to finding part values for loop bandwidth and phase margin were introduced. We now go further with this approach, considering the noise transfer functions within the loop. It is helpful to first present this in a generalized form, using the feedback tracking loop of *Figure 1*.

Example noises can be injected at various points labeled (1) to (6); we are interested in deriving the closed-loop resulting noise at any point in the loop. If we inject open-loop noise Q_{n1} into point (1), we will get a closed-loop quantity Q_{n1cl} on point (1) after the loop acts on this noise. The ratio of closed loop to open loop will be given by:

$$\frac{Q_{n1cl}}{Q_{n1}} = \frac{1}{1+G_1G_2H} = \frac{1}{1+GH} \qquad (1)$$

When the above block diagram represents a phase-locked loop, this function is the high-pass "error transfer function" $H_e(s)$ that was given in the online and long versions of Part 1. If we check any other point in the loop, where we inject noise into a node and find the ratio of closed-loop noise on that node to the injected open-loop noise, we will get the same function except for reordering of the factors G_1, G_2, and H. So:

$$\frac{Q_{nycl}}{Q_{ny}} = H_e(s) = \frac{1}{1+G_1G_2H} = \frac{1}{1+GH} \qquad (2)$$

Another critical function is the "closed-loop transfer function" CL(s) as described by Banerjee:

$$\frac{Q_{out}}{Q_{in}} = CL(s) = \frac{G_1G_2}{1+G_1G_2H} = \frac{G}{1+GH} \qquad (3)$$

The classic "phase transfer function" is given by:

$$\frac{Q_6}{Q_{in}} = H_{classic}(s) = \frac{G_1G_2H}{1+G_1G_2H} = \frac{GH}{1+GH} \qquad (4)$$

In older books, $H_{classis}$ is called simply H, whereas in more modern books, H is used for the feedback block and H = 1/N. The term $H_{classic}$ is used here to try to avoid confusion.

Note that CL(s) and $H_{classic}(s)$ look like scaled versions of H_e, but this scaling by G or GH is not flat with frequency. Because forward gain G has two integrators in a PLL (the loop filter and the VCO), the net result is that G>>1 within the loop bandwidth, and CL(s) and $H_{classic}$ are converted to low-pass form. Figures demonstrating this are shown in the full version of this article.

If we examine the noise from any point "y" into which we inject noise Q_{ny} into the loop, to an output node "z," where G_{yz} is the gain from point y to point z, we find the convenient relation:

$$\frac{Q_{nzcl}}{Q_{ny}} = \frac{G_{yz}}{1+G_1G_2H} = \frac{G_{yz}}{1+GH} = G_{yz}H_e(s) \qquad (5)$$

With this generalized information in mind, we may now consider the PLL block diagram of *Figure 2*.

The noise sources of this figure are:

V_{nx}: The steering input-referred noise of the crystal reference oscillator, from its datasheet and then modified by the VCO noise modulation function to refer to input.

$V_{nxsteer}$: The noise of the crystal steering input; for example, filtered DAC noise used to trim the crystal frequency.

V_{nxpwr}: The input-referred noise from the crystal-oscillator power supply, as described in Part 2.

K_x: Steering gain of the crystal reference in rad/sec/V. When referring noise to the crystal-oscillator input, K_x should be converted to K_{xHz}.

I_{npll}: The noise of synthesizer chip dividers and charge pump represented as a noise current, as derived in the full version.

V_{nfilt}: The output filter voltage noise density presented to the VCO steering input.

V_{nvco}: The Leeson noise of the VCO referred to its steering input.

V_{nvpwr}: The noise effect of VCO power-supply noise referred to the VCO input.

Graphs of the phase and error transfer functions are shown in the full-length version. To make use of the transfer function relationships derived above for the particular PLL case, we will need detailed filter functions. *These are given in Table 1 of the full version on the Longwing website.* With a particular filter designed and with noise sources identified, we have what we need to find the closed-loop noise. For the PLL block diagram with noise sources as given, we may write:

$$G = K_dZ_f\frac{K_o}{s} = \frac{I_{pd}}{2\pi}\frac{K_o}{s}Z_f \qquad (6)$$

The voltage noise or noise sideband to carrier (depending on whether the output node variable is in volts or in rad/sec) generated by noise "x" at point "y" is given by:

$$Q_{yz} = G_{yz}H_e = \frac{G_{yz}}{1+GH} = \frac{G_{yz}}{1+\frac{I_{pd}}{2\pi N}\frac{K_o}{s}Z_f} \qquad (7)$$

Now, we may use this relationship with the input noises to generate the rms sum of closed-loop noises on the VCO input, and then the VCO noise modulation function to give the closed-loop phase noise on the output.

From the rms sum of noises on the crystal oscillator tune input (or output), we get an open-loop phase noise on the crystal output θ_{nref}. This is divided by "R" and summed into the loop at the phase detector. The closed-loop phase noise at the (imaginary) node following feedback phase summing is $\theta_{nrefcl} = \theta_{nref}\,H_e$. We use the "magnitude" function to emphasize these are rms noise quantities. Therefore, the reference noise as modeled at the VCO input will be:

$$|V_{nxcl}| = \left|\frac{K_x}{s}\frac{1}{R}\,Z_f\,H_e\right| \qquad (8)$$

The noise from the charge pump and dividers of the synthesizer chip (often called "PLL noise") is normally handled directly at the VCO output, using methods developed by Banerjee. These methods shall be presented later, but first we will develop the method of summing all noise sources to get total phase noise.

We assume here that we have a frequency-dependent current noise function i_{npll} that can be summed into the loop filter using the transfer function approach developed above. This noise current function is derived from the Banerjee model in the full-length version. Besides allowing a unified noise-analysis approach, this new model is convenient for SPICE simulation. The noise voltage at the VCO input from the charge pump and divider noise is:

$$|V_{npllcl}| = |I_{npll}Z_fH_e| \qquad (9)$$

The closed-loop noises for the loop filter, input-referred VCO noise, and input-referred VCO power supply noise are all on

the VCO input, so they are simply the open-loop noises multiplied by H_e:

$$|V_{nfiltcl}| = |V_{nfilt} H_e(s)| \qquad (10)$$

$$|V_{nvcocl}| = |V_{nvco} H_e(s)| \qquad (11)$$

$$|V_{nvpwrcl}| = |V_{nvpwr} H_e(s)| \qquad (12)$$

It is enlightening to graph these noises separately to identify whether it is worth more effort or parts cost to reduce total noise. The magnitude of the total noise on the VCO steering input is given by the rms sum of the above sources:

$$|V_{nsteer}| = \sqrt{|V_{nxcl}|^2 + |V_{npllcl}|^2 + |V_{nfiltcl}|^2 + |V_{nvcocl}|^2 + |V_{nvpwrcl}|^2} \qquad (13)$$

Finally, this rms summed total noise voltage on the VCO input in the closed-loop state is transformed to a **total output phase noise** by:

$$L(f) = \left(\frac{S}{C}\right)^2 = \left(\frac{|V_{nsteer}| K_{Hz}}{\sqrt{2}\, f}\right)^2 \qquad (14)$$

Charge Pump and Divider Noise and Corner, Synthesizer IC Figure of Merit, and Modeling

This charge pump and divider synthesizer IC noise is often called "PLL noise." That term is avoided here, though, because confusion could arise as to whether this is one component of many, or total PLL noise. Let's coin the term "CPD noise" as an accurate alternative.

Flat Synthesizer Noise: Banerjee (Ref. 3) seems to have been the first to analyze and quantify this important noise source (Ref. 4) to useful accuracy in a way that can be specified in synthesizer datasheets. While not actually flat, inside the loop bandwidth it tends to be only a weak function of frequency. The physical source of this noise is the charge pumps and dividers. Over the years, as synthesizer ICs have become faster and pulse widths have approached zero, this noise has dropped significantly.

We can intuitively understand this noise as follows. For any given pulse width with a given jitter, we can hypothesize that there will be a floor to this noise, a term proportional to the comparison frequency (number of the narrow pulses per unit of time), and a multiplication term similar to that in multiplying the crystal-reference phase noise (note the jitter noise is at the phase-detector input, and adds to the jitter of the crystal reference). The resulting "flat" noise (not counting yet for a 1/f behavior to this CPD noise) is given by:

$$L_{flatdB}(f) = PN1HzdB + 20log|CL(f)| + 10log(f_{comp}) \qquad (15)$$

Here "PN1Hz" is the normalized floor on a per-Hz basis. It is typically given in dB, but we will have occasion to convert it to linear when adding flat and 1/f noise powers. The empirical approach supporting this equation is proven in Ref. 4, where a timing jitter analysis leads to the same results. PN1Hz is now a standard datasheet parameter.

Inside the loop bandwidth **CL(f) ~ N**, and:

$$L_{flatdB}(f) = PN1HzdB + 20logN + 10log(f_{comp}) \qquad (16)$$

Because $N = f_{out}/f_{comp}$, we may write:

$$L_{flatdB}(f) = PN1HzdB + 20log(f_{out}) - 10log(f_{comp}) \quad (17)$$

Since there's noise in each phase detector pulse, the reduction of 3 dB of in-band noise for each doubling of f_{comp} in the above relation may seem odd. Doubling f_{comp} adds 3 dB to the noise contributed by the phase detector pulses. But, doubling f_{comp} also reduces N by two, which removes 6 dB of noise multiplication. The net is the 3-dB improvement shown.

This simple equation has powerful results for the synthesizer industry. As radio designers, we are normally given f_{out}, and by using a smaller N value, we get higher f_{comp} and lower in-band phase noise while generating that f_{out}. This method is being strongly applied by semiconductor companies with modern sigma-delta fractional N synthesizers, with comparison frequencies now up to 100-200MHz (Part 4) and loop bandwidths ranging up to hundreds of kilohertz. This is key to allowing on-die VCOs to have effectively low noise at required phase-noise offsets, which despite heroic design efforts to improve their phase noise, are still significantly noisier than the best discrete VCOs (Part 4). The equation is the very heart of why fully integrated synthesizers can be sufficiently low noise for most modern applications.

Flicker Synthesizer Noise: The method adopted by Banerjee to model 1/f noise in the synthesizer chip is to assume that flicker dominates in-band noise at 10 kHz, and to scale that noise by output frequency relative to 1 GHz and by offset relative to 10 kHz. This gives:

$$L_{flickerdB}(f) = PN_{1\_fdB} + 20log\left(\frac{f_{out}}{1E9}\right) - 10log\left(\frac{f_{off}}{1E4}\right) = PN_{1\_fdB} + 20log(f_{out}) - 10log(f_{off}) - 140dB \quad (18)$$

The term PN_{1_f} is used by Analog Devices as a 1/f noise parameter and can be found in the company's datasheets. Texas Instruments refers to this same term as $PN_{PLL\_1/f}$. These are typically provided in dB form. In the equation above, the suffix "dB" is provided to make this clear.

Linear Technology uses this same basic method for specification, but eliminate references to 1-GHz carrier and 10-kHZ offset. They use the normalized 1/f noise term $L_{M(NORM-1/f)}$. Let's refer to this term with the simpler variable $PN_{flicker}$ when in linear form and $PN_{flickerdB}$ when in dB form. Their equation is:

$$L_{flickerdB}(f) = PN_{flickerdB} + 20log(f_{out}) - 10log(f_{off}) \quad (19)$$

Comparing these two equations, it is seen that:

$$PN_{flickerdB} = PN_{1\_fdB} - 140dB \quad (20)$$

$$PN_{flicker} = \frac{PN_{1\_f}}{1E14} \quad (21)$$

Combining Flat and 1/f Synthesizer Noise: To add flat power to flicker power to get a total synthesizer chip noise power, we need linear terms, which are:

$$L_{flat} = PN_{flat} = PN1Hz\,|CL(f)|^2 f_{comp} \quad (22)$$

Within the loop bandwidth:

$$L_{flat} = PN_{flat} = PN1Hz\,N^2 f_{comp} \quad (23)$$

$$L_{flicker} = PN_{flicker}\frac{f_{out}^2}{f_{off}} = \frac{PN_{1\_f}}{1E14}\frac{f_{out}^2}{f_{off}} \quad (24)$$

The total charge pump and divider noise at $f = f_{off}$ is given by:

$$L_{cpdtot} = L_{flat} + L_{flicker} \qquad (25)$$

Assuming that the flicker corner is within loop bandwidth, we may set the flicker and flat noises equal to solve for corner frequency at a particular output frequency, N, and f_{comp}. When we do this and substitute $N = f_{out} / f_{comp}$, we get as a synthesizer IC in-loop bandwidth corner frequency:

$$f_{npllcorner} = \frac{PN_{flicker} f_{comp}}{PN1Hz} = \frac{PN_{1-f}}{1E14} \frac{f_{comp}}{PN1Hz} \qquad (26)$$

There will also be a generally closer-in corner where multiplied crystal frequency will become dominant over synthesizer IC 1/f noise. Depending on the noises in question, this can range from less than 100 Hz to several kiloherz.

Current-Noise Model: The above noises are expressed on the VCO output in the closed-loop state. Synthesizer CPD noise can be expressed as a sum of a flat and 1/f noise current injected into the loop filter in parallel with a then assumed noise-free charge-pump current. This form is useful for SPICE modeling of the synthesizer noise. The analysis to determine this noise is given in the full version. The results for the combined flat and 1/f noise are:

$$i_{nplltot} = \frac{\sqrt{2}\, I_{pd}}{2\pi} \sqrt{PN1Hz\, f_{comp}} \sqrt{1 + \frac{f_{npllcorner}}{f}} \qquad (27)$$

Synthesizer IC Noise Figure of Merit: Note that a lower PN1Hz, a superior flat noise, will give a higher corner frequency for the same flicker noise profile. So, a higher corner does not necessarily denote a higher noise part. To understand when a part is actually superior, the 1/f and flat noises may be combined to give a reliable figure of merit for the total synthesizer IC noise, over a desired bandwidth f_L and with a desired phase detector frequency f_{comp}. If the synthesizer chip noise current $i_{nplltot}$ is integrated from 1 Hz to f_L, we obtain a noise power figure of merit:

$$IC_{nfom} = \frac{I_{pd}^2}{2\pi^2} f_{comp} \left(PN1Hz\, f_L + f_{comp}\, PN_{flicker}\, ln(f_L) \right) \qquad (28)$$

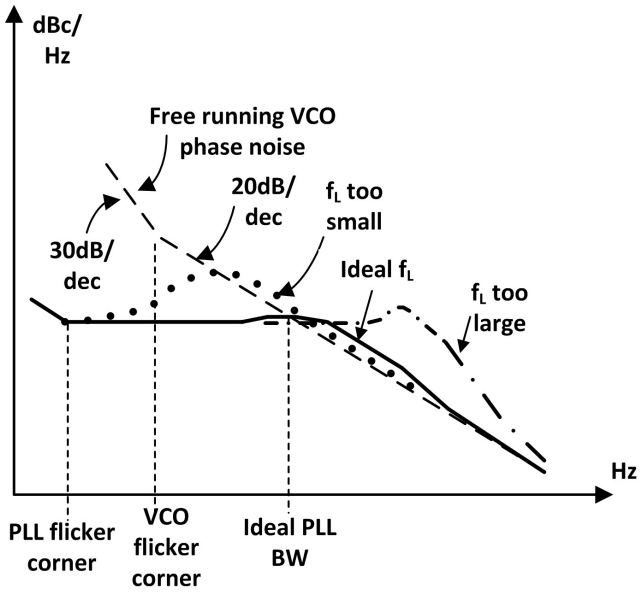
If two chips do not allow the same I_{pd} and f_{comp} to be used, then this equation with the I_{pd} and f_{comp} for each chip gives a figure of merit for noise power, where the lowest number is superior. Any time we are comparing two ICs with the same I_{pd} and f_{comp}, the figure of merit may be simplified to:

$$IC_{nfom} = PN1Hz\, f_L + f_{comp}\, PN_{flicker}\, ln(f_L) \qquad (29)$$

Optimum Loop Bandwidth Counting All Noise Sources

The "ideal bandwidth" generally means a bandwidth where the "flat" in-band noise (which will not be exactly flat) intersects the VCO free-running noise at the loop bandwidth. A lower bandwidth would mean that the VCO noise at the loop bandwidth is higher than the flat in-band noise floor that will be reached, which will look like significant noise peaking around the loop bandwidth. A higher bandwidth will mean that the noise induced by the synthesizer IC will be higher than the VCO free-running noise at the loop bandwidth. These effects are shown in *Figure 3*.

A possible limit to reaching ideal bandwidth is sigma-delta noise, which tends to peak around one half f_{comp}, and may require using a moderately lower bandwidth. However, we may use our knowledge of the noise sources to find the ideal bandwidth where the VCO plus filter noise will match the synthesizer-chip-induced noise. Because the bandwidth and noise are functions of each other, some iteration may be needed to arrive at the best possible solution.



3. Illustration of ideal bandwidth versus noise effects of too small or large a bandwidth.

Ideal Passive BW for VCO Noise and Flat Synthesizer IC Noise Only: Ignoring any noise modulation of the VCO by the loop filter and the flicker corner of the synthesizer IC, we can easily find the approximate ideal bandwidth from setting $L_{flat} = L_{VCO}$ and solving for f. This is the approach recommended by Banerjee for minimum jitter (Ref. 3, 5th edition, pp. 305-306).

Assuming the desired f_L will be on the −20 dB/dec part of the phase-noise slope, and that we know the phase noise $L(f_{ref})$ (converted from dB), the VCO noise at a frequency f_L (the desired bandwidth) will be given by:

$$P_{nvco} = L(f_{ref})\frac{f_{ref}^2}{f_L^2} = PN_{flat} \qquad (30)$$

From this ideal bandwidth, $f_{L\text{-}VCO}$, considering only VCO noise, is:

$$f_{L-VCO} = f_{ref}\sqrt{\frac{L(f_{ref})}{PN_{flat}}} \qquad (31)$$

The issues we run into with this first-order approximation are that we don't really get to perfectly maintain the free-running VCO noise due to noise modulation by filter resistors, and that the synthesizer IC flicker noise may not be negligible at the resulting bandwidth. We can usually use sufficiently low power-supply noise whereby supply noise modulation is negligible, as very-low-noise integrated regulators have become recently available; if they won't do, then still lower noise can be provided by discrete solutions (Part 4). However, the filter noise will usually be at least noticeable and at least moderately alters the free-running VCO noise.

Ideal BW with the Passive Loop Filter Including Synthesizer and VCO Flicker Noises: We get a more accurate measure of the optimum minimum jitter bandwidth when these noise sources are taken into account. Such noise sources may lead to either an *increase or decrease* in ideal bandwidth to that predicted using VCO noise alone. Adding loop filter noises and VCO flicker noises will push out the ideal bandwidth. But, counting in the higher synthesizer IC noise with synthesizer flicker tends to push toward a lower intersection. In a particular case, either one of these may dominate. There are also noise terms from the crystal-reference oscillator, but these will usually be negligible until lower offsets, as they come to dominate the locked noise on the order of 50 Hz (ovenized super-low-noise reference) to about 3 kHz (mobile handset class VCTCXO). The crystal noise would tend to push to a lower locked bandwidth as ideal.

When we consider ideal bandwidth with the noise of a filter added to the VCO noise, in the frequency range where the bandwidth f_L will fall on the −20 dB/dec part of the VCO phase noise, and take account of synthesizer flicker noise, we may write:

$$P_{nvco} + P_{nfilt} = L_{flat} + L_{flicker} = PN1Hz\,N^2 f_{comp} + PN_{flicker}\frac{f_{out}^2}{f_L} \qquad (32)$$

For the passive filter, the noise comes from the resistors in the filter. We are mostly interested in the noise at the loop bandwidth, where it's neither suppressed by the loop or filtered off by higher-order poles. At this frequency, using the thermal noise and the VCO noise modulation function:

$$P_{nfilt} = \frac{M4kTR_2K_{Hz}^2}{2f_L^2} \qquad (33)$$

In this equation for P_{nfilt}, "M" is a multiplier for filter form. M = 1 for the first- and second-order filter (only R_2); M is generally about 2-3 for the third-order form (adding R_3); and M is generally about 3-4 for the fourth-order form (adding R_3 and R_4). Now, we can get a good approximation for R_2 from the second-order PLL equations, where:

$$R_2 \cong \frac{2\pi N f_L}{K_{Hz}I_{pd}} \qquad (34)$$

Substituting this into the equation for passive filter noise:

$$P_{nfilt} = \frac{M4\pi kTNK_{Hz}}{f_L I_{pd}} \qquad (35)$$

We may substitute this relation for P_{nfilt} and the linear expressions for P_{nvco} and PN_{flat} into Equation 32, and solve for ideal bandwidth f_L. Because the expression for P_{nvco} as a function of frequency is second order, the expression for P_{nfilt} is first order, and the expression for P_{nflat} is constant, we end up with a quadratic equation:

$$P_{nflat} f_L^2 - \left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2 \right) f_L - L_{vco}(f_{ref}) f_{ref}^2 = 0 \quad \textbf{(36)}$$

In this quadratic equation, f_{ref} is not the phase detector frequency f_{comp}, but the point on the −20 dB/dec part of the VCO slope where we get an example measure of VCO phase noise. Here, 10 kHz is most commonly used, but if the VCO flicker corner is not well below 10 kHz, then a higher reference frequency should be chosen. Now, solving for ideal f_L, we of course get:

$$f_L = \frac{\left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2 \right) \pm \sqrt{\left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2 \right)^2 + 4P_{nflat} L_{vco}(f_{ref}) f_{ref}^2}}{2P_{nflat}}$$

(37)

This solution will always have a positive and negative frequency result, so there's never any doubt as to the correct root.

Note in the above that it was assumed that the final bandwidth was at a frequency greater than the VCO flicker corner. This is often—but not always—true. If the final bandwidth calculated using the above is in fact below the VCO flicker corner, then we must modify our design procedure. This is done by noting that for frequency f_L below the flicker corner f_{cvco} of the VCO, we have a more complicated equation for VCO free-running phase noise:

$$P_{nvco} = L(f_{cvco}) \frac{f_{cvco}^3}{f_L^3} + L(f_{ref}) \frac{f_{ref}^2}{f_L^2} \quad \textbf{(38)}$$

Now when this relation for VCO phase noise is used to find f_L, we get a cubic relationship that needs to be solved numerically:

$$P_{nflat} f_L^3 - \left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2 \right) f_L^2 - L_{vco}(f_{ref}) f_{ref}^2 f_L - L_{vco}(f_{cvco}) f_{cvco}^3 = 0$$

(39)

Ideal Bandwidth for the Slow Slew Active Loop Filter: This inverting form loop filter is the most recommended for those cases where the better medium and far out noise of a low-noise, high-tune-range discrete VCO is worth the extra cost and board area. An expression for the noise terms in the output of this filter was derived in Part 2 (Ref. 2).

Since we're concerned with the noise at the loop bandwidth when deriving ideal bandwidth, we can leave off the term for the noise of R_3. This noise is negligible at the loop bandwidth because the input pole is well above the bandwidth, the backward impedance is much greater than the forward impedance, and thus the noise gain relative to this term is <<1. Similarly, R_4 can be of such low value relative to R_2 that we can neglect its noise as well for the purpose of finding bandwidth. We will also assume that VCO supply noise has been made low enough to be negligible (see Part 4). Thus, the filter noises we use are:

$$V_{noptot}^2 = G_{n1}^2 V_{np}^2 + V_{nopR2}^2 + V_{nopInop}^2 \quad \textbf{(40)}$$

Recall in the above that V_{np} is the combined op amp and reference noise. G_{n1} is the noise gain for the op amp plus input, which will usually be a small number in the range of about 1.005 to 1.02. It will be nailed down once the loop bandwidth and loop filter are fully defined. Next, we translate this noise to VCO output using the VCO noise modulation function, which gives:

$$P_{nfilt} = \frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2f_L^2} + \frac{4\pi kTNK_{Hz}}{I_{pd} f_L} + \frac{i_{nop}^2 2\pi^2 N^2}{I_{pd}^2} \quad \textbf{(41)}$$

We recall the VCO noise including noise below its flicker corner as:

$$P_{nvco} = L(f_{cvco}) \frac{f_{cvco}^3}{f_L^3} + L(f_{ref}) \frac{f_{ref}^2}{f_L^2} \quad \textbf{(42)}$$

The main equation to use if setting VCO and filter noise equal to synthesizer IC noise at the loop bandwidth f_L is:

$$P_{nvco} + P_{nfilt} = L_{flat} + L_{flicker} = PN1Hz\, N^2 f_{comp} + PN_{flicker} \frac{f_{out}^2}{f_L} \qquad (43)$$

The above equations may be combined to give this equation cubic in f_L:

$$\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat} \right) f_L^3 + \left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2 \right) f_L^2 + \left(\frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2} + L_{vco}(f_{ref}) f_{ref}^2 \right) f_L + L_{vco}(f_{cvco}) f_{cvco}^3 = 0 \qquad (44)$$

Here, the noise gain G_{n1} from op amp plus input to op amp output at the loop bandwidth is given by:

$$G_{n1}^2 = \frac{V_{nopp}^2}{V_{np}^2} = \left| 1 + \frac{Z_{for}}{Z_{back}} \right|^2 \cong 1 \qquad (45)$$

The expressions for Z_{for} and Z_{back} developed in the full-length version of Part 2 may be approximated at f_L as:

$$Z_{back} = R_3 + \frac{1}{sC_3R_3} = \frac{sC_3R_3+1}{sC_3} \cong \frac{1}{j2\pi f_L C_3} \; (at\, f_L) \qquad (46)$$

$$Z_{for} = \frac{1+sR_2C_2}{s(C_1+C_2+sR_2C_2C_1)} \cong R_2 \; (at\, f_L) \qquad (47)$$

To the author's knowledge, the above cubic relationship for f_L is the most accurate published relationship for getting an initial value for ideal loop bandwidth, as it takes all of the major factors into account. However, it still relies on several approximations, which are discussed in the full-length version along with more detailed analysis recommendations.

If we ignore the VCO flicker corner on the assumption the loop bandwidth exceeds the VCO corner, then the cubic equation reduces to:

$$\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat} \right) f_L^2 + \left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - PN_{flicker} f_{out}^2 \right) f_L + \left(\frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2} + L_{vco}(f_{ref}) f_{ref}^2 \right) = 0 \qquad (48)$$

Ideal Bandwidth for the Semi-Active Buffered Loop Filter: The ideal bandwidth for this filter form is analyzed in the full-length version, available on the publications page at www.longwingtech.com.

SPICE Modeling of Synthesizers and Their Noise

SPICE and similar CAD modeling is, of course, one of the greatest advances in electronic design history, allowing for excellent results when component models are accurate. The mathematical analysis is more flexible than SPICE, but it's quite a chore to juggle all of the noise sources and control system behaviors described above. Handling this mass of data can easily lead to making mistakes.

A SPICE analysis can confirm the correctness of the mathematical analysis, and often be more accurate. Doing both for cross-checking and then having each analysis form available to take advantage of their particular strengths gives designers the best of both worlds. Methods for using SPICE in PLL noise analysis are provided in the full version.

Spur Noise

Spurs are discrete frequency components most commonly caused by digital noise on the phase detector output; they get through the loop filter in at least noticeable form and cause modulation on the input of the VCO. These "modulated" spurs are thus symmetrical about the carrier. "Direct" spurs also exist. For instance, reference or clock noises that leak around the loop filter are present in ground plane noise, or come in through the power supply. These are discussed in the full version, and in greater detail in the references given there.

System Phase-Noise Requirements

This article series will not take the space to derive system requirements of multiple systems in high detail. However, as such requirements are seldom given in synthesizer text books, some approximate example requirements are derived in the full-length version.

Summary

In recent years, synthesizer IC noise has been drastically reduced, and, in turn, the architectural advances of high-bandwidth sigma-delta synthesizers has allowed outstanding in-band noise suppression. Lower noise and higher-frequency references that further support low in-band noise are also becoming available at outstanding cost reductions compared to the price of low-noise ovenized references. In this situation, even the noise of on-die VCOs can be suppressed to the point of allowing fully integrated synthesizers to address most applications, at least for lower offset frequencies. Discrete VCOs still retain their classic noise advantages at higher offsets, and in some cases remain the optimum solution.

Key parts and their noise behaviors will be reviewed in Part 4. The examples in Part 5 will explore how the advantages of discrete VCOs could be combined with the latest sigma-delta synthesizer technology to allow discrete VCOs to regain their historical advantages. This would require that discrete VCOs be extended to higher frequencies while retaining their higher Q and higher tune range advantages over integrated VCOs. It remains to be seen if this situation will develop.

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