DESIGN

Constructing Circuits For Short-Range Radios

Builders of short-range radio links must pay attention to different performance requirements and cost issues when selecting a technology for a particular product design.

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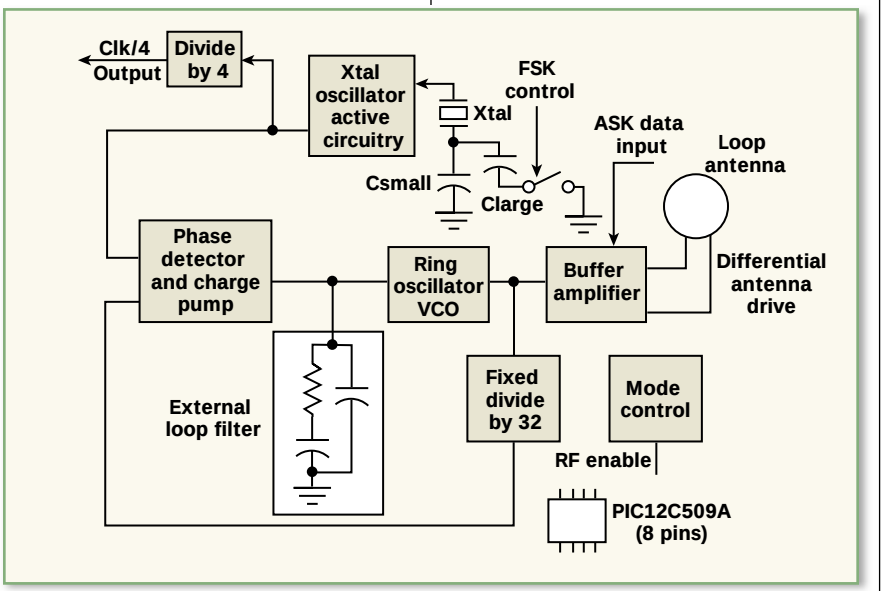
Short-range-radio designers generally do not share the resources available to the more standardized segments of wireless communications, such as cellular systems. For one thing, reference material on short-range radios is limited. To aid designers, Part 3 of this article series on short-range radios will review options for implementing short-range radios. The first two parts of this series have discussed system design issues (see *Microwaves & RF*, September 2001, p. 73) and regulations (see *Microwaves & RF*, October 2001, p. 79), respectively.

The lowest-cost option for short-range radio equipment is the classic inductive-capacitive (LC) link. This approach is acceptable in the US and other Federal Communications Commission (FCC)-based countries, but not in Europe with its tighter requirements for frequency accuracy. For European systems, surface-acoustic-wave (SAW) links are the lowest-cost systems that can generally meet those more stringent

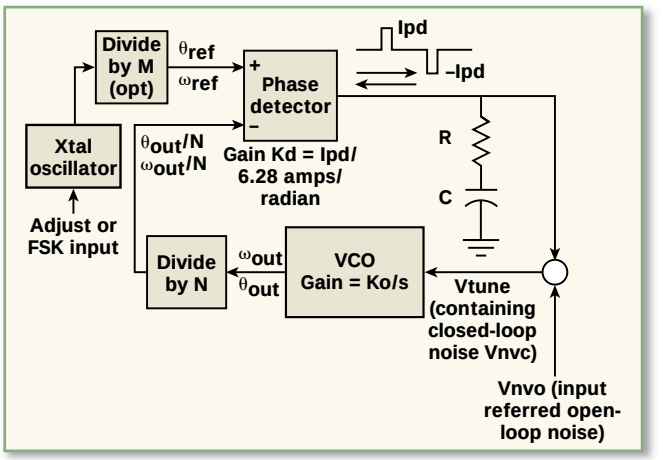


3. The model rfPIC12C509 is a PLL-based 310-to470-MHz short-range transmitter with integrated microcontroller.

requirements. The better frequency accuracy of SAWs compared to LC circuits supports narrower bandwidth receivers (Rxs) with improved sensitivity and interference immunity. This improved performance with good cost efficiency has led to SAWs being the method of choice over the last decade for wireless remote-keyless-entry (RKE) applications. However, within the last few years, integrated-circuit (IC) phase-locked-loop (PLL)-based systems have challenged SAWs in cost while providing an improvement in performance. This improvement is again partly based on better frequency accuracy, supporting narrower band and, thus, improved Rxs. Frequency synthesis also enables software-controlled frequency agility. The introduction of microprocessors into the links supports error control, transmit-power-level control, microcellular handoff, and a host of other features for more complex data-communications applications.

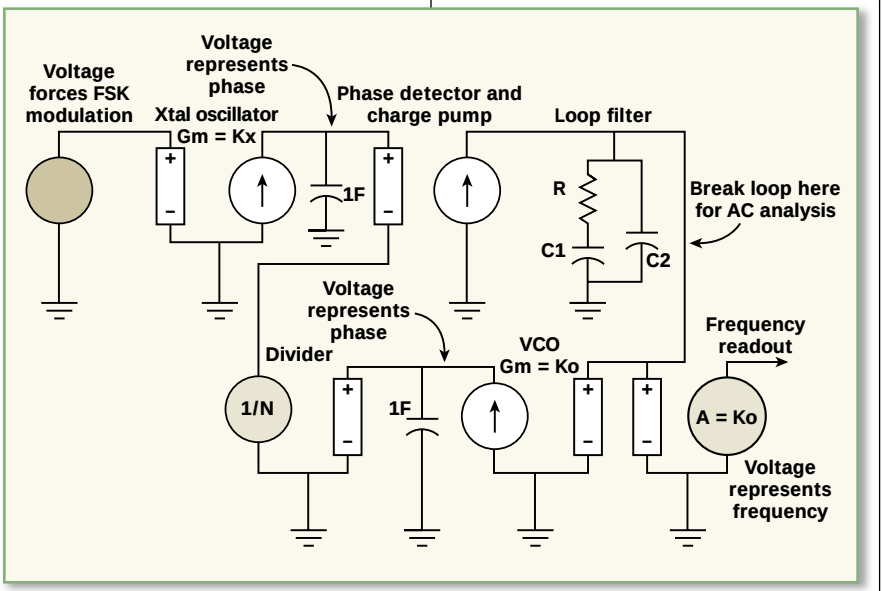
For example, the model rfPIC12C509 from Microchip Technology is a PLL amplitude-shift-keying (ASK) [18 pin SOIC 509AG version] and frequency-shift-keying (FSK) [20-pin SSOP 509AF version] transmitter (Tx) with integrated PICmicro® controller that is typical of this class of Tx **(Fig. 3).** Using the recommended board-level implementation, acceptable phase-noise performance, carrier-frequency accuracy, and transmitted harmonic suppression can be achieved.

The design of PLLs is generally not trivial, and has inspired entire books (refs. 4-6). However, most references do not provide coverage of the most popular "current pump" form of PLL, and instead focus on the older active (optical-amplifier-based) loop-filter forms (with the exception of ref. 5). The advantages of the current-pump form include not only saving an optical amplifier, but also the lower phase noise due to the fact that the current pump is only on for a tiny fraction of the time in the locked state, thus greatly reducing flicker noise on the controlling input to the voltage-controlled oscillator (VCO), and, thus, limiting induced phase noise. Some short-range Tx ICs include the loop filter on the die and the customer need not understand or design a PLL. Others, such as that on the rfPIC12C509, provide more flexibility by using an off-die loop filter that a user can either design or take from an applications note. Of course, an RF IC designer must have a thorough understanding of the subject.



4. This block diagram shows a basic second-order charge-pump PLL.

Since they are not commonly available, the design equations for current-pump PLLs have been collected here. They may be developed by applying standard control-system frequency-domain analysis, and the same basic methods will be used later in analyzing closed-loop noise. In applying this type of analysis to PLLs, the variations of voltage, frequency, and phase in the frequency domain are studied as small-signal variations around an operating point (the locked frequency). It may seem odd to view frequency and phase variations in the frequency domain, but it is perfectly valid. In this analysis, a VCO is viewed as an integrator of input voltage to output phase. This is also initially confusing, but it follows directly from the definition of radian frequency being the time derivative of phase. With these points in mind, the system is examined as a feedback-control system, which remains stable if the phase shift around the total loop is less than 360 deg. at all frequencies where the loop gain is greater than 1. It is also common for the simple analysis of PLLs to be put into what is known as "second-order normalized form." In this standard form, loop parameters may be more easily viewed and understood, and loop-component values can be calculated from



5. This basic closed-loop PLL SPICE model can be used for transient-response analysis.

Table 4: Tuning curves for an IC VCO

FREQUENCY (MHz)	K_0 (MHz/V)
310	225
320	253
330	275
340	291
350	306
360	319
370	323
380	323
390	313
400	294
410	274
420	244
430	211
440	177.5
450	144.6
460	113.2
470	78.9

the desired loop parameters. The loop parameter of interest are the natural frequency, ω_n, and the damping factor, ξ. The natural frequency is the frequency at which the loop "rings" when settling. Though related to open-loop unity gain bandwidth, the two terms are not the same. The damping factor provides a measure of phase margin and stability. The loop is stable if $\xi > 0$, and it has the fastest settling time if $\xi = 0.707$. It does not noticeably ring if $\xi > 1$, but it does overshoot on step inputs since the phase margin is always less than 90 deg. Since extra filtering with additional phase shift is common in PLLs (this makes them higher than second order and thus not amenable to standard normalized form), a common design practice is to set $\xi = 1.0$ to 1.5 for hand calculation, and then adjust components in simulation to optimize phase margin, settling time, and spurious suppression. A simplified but usefully accurate Simulation Program with Integrated Circuit Emphasis (SPICE) model for higher-order PLL simulation will be shown for these simulations.

Figure 4 shows the block diagram of a suitable second-order current-pump PLL (for now, ignore the noise voltages V_{nvo} and V_{nvc} which will be used in a later noise analysis). It is suitable in that the sampling nature of the loop will be ignored, and the analysis performed using continuous variables. This is valid as long as the loop bandwidth is a very small fraction of the sample rate, but detailed simulation to determine actual phase shift is required when loop bandwidths are a significant (greater than a few percent) fraction of sample rate (reference frequency at the phase-detector input). The loop can maintain good stability with a loop bandwidth up to approximately 10 percent of the sample rate, though 5 percent is a safer number. The loop consists of a reference-frequency source, a VCO, a frequency divider, and a phase detector.

The reference-frequency source is almost always a crystal oscillator, which may be followed by an optional fixed or programmable divider of value "M." The purpose of the PLL is to force the VCO frequency to be some exact multiple of the reference frequency, thus transferring the high

accuracy and quality of the crystal oscillator to a frequency higher than that at which crystals may directly operate.

The VCO block converts an input "steering" or "tuning" voltage into an output frequency and phase. The VCO on the rfPIC12C509 is a relaxation oscillator, as opposed to the higher quality-factor (Q) LC or resonant oscillators that are common in standard radios. The high loop bandwidth supported by the fixed divider and high reference frequency suppress the "phase noise" of the low-quality free-running relaxation oscillator, thus allowing the use of a completely integrated VCO with limited performance. The "gain" of the VCO is normally referred to as K_0 and for PLL design normally has units of radians per second per volt (but often used in Hertz per volt form for noise calculations). Since the analysis is of phase variation and the VCO integrates input voltage to output phase (frequency offset from desired lock "integrates" into a phase error), the control-system frequency-domain transfer function of the VCO is K_0/s. Similar to most VCOs, the VCO in the rfPIC12C509 does not show perfect linearity. It varies over frequency **(Table 4)**, and this variation must be taken into account in the design of the PLL to ensure that desired loop parameters are achieved while stability and noise performance are maintained.

The digital frequency divider simply divides down the VCO frequency to match the reference frequency. In a frequency-agile synthesizer, this would be a programmable element. The divider reduces frequency and phase by its transfer function 1/N.

Phase Detector

The phase detector is almost always a digital subsystem that compares a reference frequency to the divided VCO output, producing a pulse width equal to the time difference between these signals. In the locked state there is no phase difference, so this width approaches zero. In the case of an active loop filter, the phase-detector output voltage directly drives the loop filter. For the current-pump case, the phase-detector output turns transistor-current sources on and off. These current pumps are then actually part of the phase detector, so that the current-pump phase-detector output is in current per radian of phase-error input. It is a sampled encoding but happens so quickly that continuous approximation is valid for basic analysis. The phase detector will provide a current, I_{pd}, for a time representative of up to 2π radians of phase error before the phase detector "rolls over" (runs out of encoding range by infringing into the next sample time). Its "gain" is therefore $K_d = I_{pd}/2\pi$ A/radian.

The loop filter takes the current pump output currents and, through filtering, suppresses their high-frequency content at the sampling rate and simultaneously converts the current back into a voltage to drive the VCO. A difference in the analysis of current pump versus optical-amplifier active loop-filter PLLs is that the active loop filter is a voltage-to-voltage transfer function, and the current-pump form is a current-to-voltage transfer function. The transfer function is simply the impedance of the loop filter, so since it is in its simplest form a series RC circuit in parallel with the phase-detector output, its transfer function is F(s) = (sRC + 1)/sC.

The phase transfer function of the loop is defined here as:

$$H(s) = \left(\theta_{out}/N\right)/\theta_{ref} \qquad (19)$$

where:

H(s) = the transfer function from the reference input on the phase detector to the feedback input.

$$H(s) = \left[\left(K_0 I_{pd} R\right)/(2\pi N)\right]s + \left[\left(K_0 I_{pd}\right)/(2\pi NC)\right]/s^2 + \left[\left(K_0 I_{pd} R\right)/(2\pi N)\right]s + \left[\left(K_0 I_{pd}\right)/(2\pi NC)\right] \qquad (20)$$

Table 5: Loop-filter values and loop parameters

R	C1 (pF)	C2 (pF)	FREQ. (MHZ)	K_0 (MHz/V)	LOOP BW	PHASE MARGIN	TRANSIENT OVERSHOOT	COMMENT
680	390	0	315	239	220 kHZ	73	31 percent	2nd order for reference Nat. frequency = 112 kHz Damping = 0.94
680	3900	390	315	239	190 kHZ	55	46 percent	Set up for U.S.
680	3900	680	315	239	175 kHZ	47	58 percent	
680	3900	1000	315	239	155 kHZ	39	76 percent	Note increasing overshoot with decreasing margin
680	3900	390	380	323	250 kHZ	54	45 percent	
680	3900	390	470	79	80 kHZ	45	67 percent	
1000	3900	0	434	198	260 kHZ	77	22 percent	Set up for European
1000	3900	390	434	198	220 kHZ	52	40 percent	Last narrow BW
7500	39	0	315	239	2.5 MHz	59	26 percent	Wide BW, nat. freq. = 1.13 MHz,-Damping = 1.03
7500	39	4.7	315	239	2.1 MHz	37	46 percent	
10K	39	0	434	198	2.85 MHz	57	20 percent	Nat. frequency. = 1 MHz, Damping = 1.25
10K	39	4.7	434	198	2.15 MHz	31	48 percent	
10K	39	4.7	434	198	2.15 MHz	31	0 percent	Square-wave modulation filtered with 100-kHz pole

This will turn out to be a lowpass function, and one that is highly indicative of loop locking, tracking, and noise behavior. From Fig. 3, the result of solving for this relationship is:

[SEE EQ. 20 ON PG. 66]

The standard normalized form of the second-order system is provided by:

$$H(s) = \left(2\varsigma\omega_n s + \omega_n^2\right) / \left(s^2 + 2\varsigma\omega_n s + \omega_n^2\right) \quad (21)$$

[SEE EQ. 21 ABOVE]

The two equations are in the same form, and by equating terms, the following analysis equations are obtained:

$$\omega_n = \left[\left(K_0 I_{pd}\right) / \left(2\pi NC\right)\right]^{0.5} \quad (22)$$

$$\varsigma = \left(K_0 I_{pd} R\right) / \left(4\pi N\omega_n\right) \quad (23)$$

Referring to Fig. 4, the common PLL error-transfer function is defined as:

$$H_e(s) = \left(\theta_{out} / N\right) / \theta_{ref} \quad (24)$$

Similar analysis shows that $H_e(s)$ may also be represented in normalized form as:

$$H_e(s) = s^2 / \left(s^2 + 2\varsigma\omega_n s + \omega_n^2\right) \quad (25)$$

where:

$H_e(s)$ = a highpass function.

However, the phase transfer function, H(s), is a lowpass function. It will turn out that many of the modulation and noise responses of PLLs can be conveniently expressed using these functions, which is a fact that is not highlighted in standard references.

From Eqs. 22 and 23, it is possible to obtain:

$$C = \left(K_0 I_{pd}\right) / \left(2\pi N\omega_n^2\right) \quad (26)$$

$$R = \left(4\pi N\omega_n\varsigma\right) / \left(K_0 I_{pd}\right) \quad (27)$$

Equations 26 and 27 are used to determine R and C based upon chosen values for the natural frequency and the damping factor. In practice, a second capacitor is normally added in parallel with the series RC of the suitable second-order loop filter, converting the loop to third order and adding additional phase shift.

The design equations for the basic second-order PLL model will provide a design that is close to the desired results. However, there are almost always additional poles in the loop that add phase shift that must be taken into account. A simple SPICE model is the easiest way to attack analysis of these effects and to obtain time-domain responses. **Figure 5** shows this model, where the sampling nature of the loop is neglected. The model is based on representing phase as voltage. The inte-

grating action of VCOs as integrators from input voltage to output phase is performed by current sources driving capacitors. To make this analogy mathematically correct, note that the output phase of a VCO is provided by:

[SEE EQ. 28]

$$\theta_{out}(t) = \int_0^t \omega(t)dt = K_0 \int_0^t V_{in}(t)\,dt \quad (28)$$

The voltage on a capacitor driven by a voltage-controlled current source is:

[SEE EQ. 29]

$$V_{out}(t) = (1/C)\int_0^t i(t)dt = (g_m/C)\int_0^t V_{in}(t)dt \quad (29)$$

If the capacitance is 1 F, then by setting $g_m = K_0$, the VCO may be replaced with the current source driving a capacitor, with output voltage numerically equal to VCO phase. This has been performed in Fig. 5 with two such integrators representing a voltage-controlled-crystal-oscillator (VCXO) reference and the VCO. The current pump uses the actual value the chip provides (260 µA in the case of the rfPIC12C509), and the divider is represented as the fraction used (1/32 in the case of the rfPIC12C509). Since the bandwidth of this PLL type usually exceeds 100 kHz, it can track crystal-oscillator frequency variations to the limit that the crystal can be modulated. In the rfPIC12C509 the crystal is modulated by varying the capacitance in series with the crystal. This effect is modeled in Fig. 5 by a voltage-driven VCXO. If the crystal oscillator is pushed near the limit of its modulation bandwidth (approximately 10 to 15 kHz), then its response to modulation is complex, though basically low-pass and thus amenable to modeling using filtering preceding the VCXO block of Fig. 5. The crystal oscillator of the rfPIC12C509 can typically be modulated up through 20 kb/s. Since loop filters are typically designed to support PLL operation for noise and lock time, and not for response to FSK modulation of the PLL, some modifications of typical design parameters are called for in setting up the PLL for FSK modulation. Generally, a larger-than-normal damping factor (more phase margin than the typical 45 deg.) is used. This Tx also provides for ASK modulation through turning the power amplifier (PA) on and off, in which case the standard choices for damping factor and phase margin apply. Generally for ASK a damping factor of 0.7 (45 deg. of phase margin) will provide the fastest settling time while providing acceptable tran-

sient response and minimum lock time (approximately $2/f_n$, where f_n is the natural frequency).

Using the SPICE model, a set of values for loop filters were generated for the rfPIC12C509 **(Table 5)**. Some interesting trends may be observed here. First, the significant difference between loop bandwidth as defined by the open-loop unity-gain crossover and the natural frequency as observed in common PLL design is evident. The loop bandwidth is typically several times the natural frequency, and unlike the natural frequency, the loop bandwidth is not independent of the damping factor. However, as the damping factor approaches zero (as loop-resistor R approaches zero), the loop bandwidth will approach the natural frequency. The damping resistor pushes the loop bandwidth higher because the charge-pump current flowing through it induces a greater voltage as R increases, and, thus, greater loop gain. The additional capacitor (C2) necessary to suppress synthesizer spurious offset from the carrier by the loop sample rate pushes loop bandwidth and phase margin back down.

FSK Modulation

FSK modulation within a PLL can be provided by several methods. The simplest practical method that can provide modulation down to DC is to modulate the reference, as is performed with the rfPIC12C509. In this IC, FSK modulation is implemented by keying a capacitor in series with the crystal, so it is shaped only by the natural response of the crystal (to be covered in detail in Part 5 of this article series). The wideband PLL then follows this modulation, which is easily performed since it is so much wider than the data bandwidth that the crystal will support (20 kb/s). However, the PLL will generate undesired overshoot with step modulation. The data in Table 5 shows that a decrease in loop-phase margin will increase the overshoot of the VCO frequency output. Overshoots to 50 percent of peak FSK are common if steps are not taken to control it. The primary step taken by the user of this part is to maintain the greatest phase margin consistent with meeting spurious requirements (see the previous part of this article series). This is aided by the fact that the crystal response cannot actually make a sharp step. It is a complex lowpass filter function that does not exhibit an instant transition. The last row in Table 5 shows the large difference in step response that occurs when the modulating signal is even lightly filtered, as long as the filtering is well-below the loop bandwidth. In that row, FSK occurs at 10 kb/s, and is filtered with a first-order lowpass filter with pole at 100 kHz with a loop bandwidth of 2.15 MHz. The loop is so fast that it tracks the changing reference almost perfectly, and, hence, does not overshoot. This mild filtering, which is built into the crystal, accounts for the difference between severe overshoot of 48 percent of peak value and overshoot of less than 1 percent.

Analytically, it may be easily shown that the transfer function from reference-frequency input to VCO fre-

quency output is also provided by the phase-transfer function of Eq. 21. If the frequency response of the crystal to a modulating input is $V_m(s)$, then the transfer function from $V_m(s)$ to the VCO output frequency is provided by:

$$\omega_{out}(s) = V_m(s)X(s)H(s) \quad (30)$$

Response $V_m(s)$ may be replaced with another signal type, such as the step-function-modulated capacitance used in the rfPIC12C509. Transfer function X(s) may be crudely modeled as a first-order lowpass response, and simulations will show that this will greatly reduce the overshoot of the FSK as long as the loop bandwidth exceeds the crystal-modulation bandwidth.

Phase-Noise Control

Phase-noise control in VCOs is a subject that has been well-covered in previous work, but there are some new twists with respect to short-range radios. Phase noise is a particular problem in short-range radio because phase-noise performance is not specified in standards, and due to the low power consumption and low Q of integrated VCOs. Some of these VCOs do not use bandpass resonators, and are effectively relaxation oscillators with a bandwidth from DC to beyond the oscillation frequency. Their Q is approximately 1, as opposed to the loaded Q of 10 to 50 that could be attained with an LC oscillator. Since phase noise is inversely proportional to Q^2, the phase noise of these oscillators is particularly poor. This problem is typically dealt with by use of a wide-bandwidth PLL, which suppresses close-in phase noise to approach the multiplied phase noise of the crystal-reference oscillator. This also suppresses phase noise induced by other sources, such as flicker and digital noise on the power supply of the VCO and PLL. How wide must the PLL loop bandwidth be? A procedure to answer this critical question will be provided next month in the fourth part of this article series on short-range radio design.

Next month, Part 4 of this series will compare the phase-noise characteristics of different frequency sources, including a crystal oscillator, a free-running VCO, and a phase-locked VCO. A phase-noise analysis will be provided to understand the effects of noise on receiver bit-error-rate (BER) performance for different data formats. MRF

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