Noise and its Shaping in Ultra-Low Noise Synthesizer Design

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Introduction

This is the third article in our low noise synthesizer design series, and is the full length version. The shorter print version was published in "Microwaves & RF" magazine in March, 2019, and the medium length digital version simultaneously published on their website. The first article in this series (Dec. 2018) covered basic design for functionality and stability. The second article (Feb. 2019) covered the many noise sources in the synthesizer outside of the actual synthesizer IC. This third article covers synthesizer IC noise, the closed loop shaping of noises, and related issues such as optimum bandwidth. A key metric for characterizing synthesizer IC noise is developed. Additional material given only in this long version includes derivation of charge pump noise in current form, spur noise, SPICE modeling of PLL noise, and applications noise requirements. The fourth article will review parts and tools available to the low noise synthesizer designer. The concluding fifth article will present low noise design examples. We will defer issues of noise coupling in the layout and microphonic noise suppression to future publication.

Recent years have seen major changes in the frequency synthesis art. Ultra-low noise discrete VCO's, which still enjoy a 20-30dB phase noise superiority over the best integrated VCO's, are no longer always the preferred solution. Integrated VCO's are now paired with sigma delta fractional N architectural innovations that often allow them to have not only surprisingly good noise performance, but often superior performance, particularly for applications where closer in phase noise is the issue. The ways this is achieved may be understood from the noise shaping material in this article. An example illustrating how discrete VCO design can be extended to use these same methods to maintain its superior performance will be given in article 5. Superior Q at frequency matching the high frequency of on-die VCO's, if coupled with equivalent synthesizer IC noise in the discrete VCO case and low noise loop filter design, would allow the lowest total noise of all.

The material presented here also leads directly to analysis of optimum loop bandwidth taking all significant noise sources into account, which is a key design topic that to the author's knowledge is not published elsewhere.

Noise Transfer Functions and Total Synthesizer Noise

The previous article described the main open loop noise sources in the PLL. Now, we turn our attention to how these noises are shaped *by* the PLL into the closed loop noise. A fundamental feature of the modern, high bandwidth PLL is that the very low noise of the input crystal reference is transferred to the VCO, for frequencies within the loop bandwidth, down to the noise floor allowed by the synthesizer IC's own noise (dividers and charge pump). Beyond the loop bandwidth the VCO reverts to its own free running noise, hopefully only slightly degraded by filter and power supply noise.

In article 1 of this series, particularly the long version, the transfer functions pertinent to fining part values for loop bandwidth and phase margin were introduced. We now go farther with this approach, considering the noise transfer functions within the loop. It is helpful to first present this in a generalized form, using the feedback tracking loop of Figure 1.

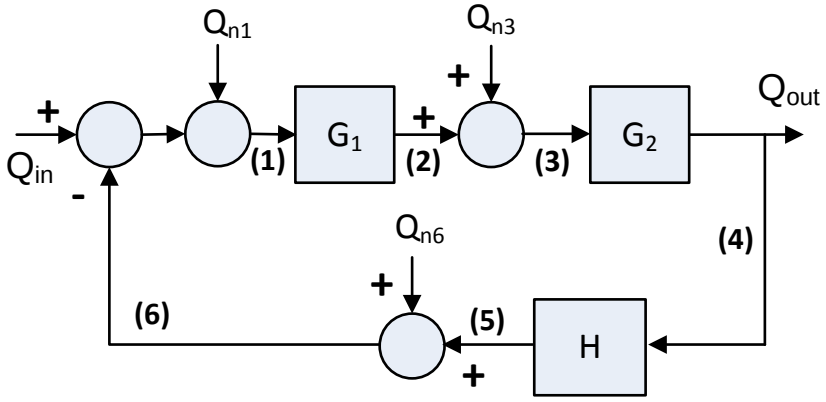

Figure 1: A generalized feedback tracking loop with noise injected at various spots is useful for deriving the noise transfer functions from a point "y" to a point "z". The forward gain G is here broken up into G_1 and G_2 for generality.

In this generalized loop we use the generalized quantity "Q" to emphasize that variables can be in the form of voltage, current, phase, frequency, or other forms. Example noises can be injected at various points labeled (1) to (6), and we are interested in deriving the closed loop resulting noise at any point in the loop.

If we inject open loop noise Q_{n1} into point (1) we will get a closed loop quantity Q_{n1cl} on point (1) after the loop acts on this noise. The ratio of closed loop to open loop will be given by:

Equation 1: $$\frac{Q_{n1cl}}{Q_{n1}} = \frac{1}{1+G_1G_2H} = \frac{1}{1+GH}$$

When the above block diagram represents a phase locked loop, this function is the "error transfer function" $H_e(s)$ that was given in the long version of article 1. $H_e(s)$ turns out to be a high pass function, with final high pass corner at the loop bandwidth. If we check any other point in the loop, where we inject noise into a node and find the ratio of closed loop noise on that node to the injected open loop noise, we will get the same function except for reordering of the factors G_1, G_2, and H. So:

Equation 2: $$\frac{Q_{nycl}}{Q_{ny}} = H_e(s) = \frac{1}{1+G_1G_2H} = \frac{1}{1+GH}$$

Another critical function is the "closed loop transfer function" as described by Banerjee, which is a scaled version of the "phase transfer function" as described by Best, Gardner, and other authors of classic phase locked loop books. The closed loop transfer function CL(s) is given by:

Equation 3: $$\frac{Q_{out}}{Q_{in}} = CL(s) = \frac{G_1G_2}{1+G_1G_2H} = \frac{G}{1+GH}$$

The classic "phase transfer function" is given by:

Equation 4: $$\frac{Q_6}{Q_{in}} = H_{classic}(s) = \frac{G_1 G_2 H}{1+G_1 G_2 H} = \frac{GH}{1+GH}$$

In older books $H_{classis}$ is called simply H, whereas in more modern books H is used for the feedback block and H = 1/N. The term $H_{classic}$ is used here to try to avoid confusion.

Note that CL(s) and $H_{classic}(s)$ look like scaled versions of H_e, but this scaling by G or GH is not flat with frequency. Because forward gain G has two integrators in a PLL, the net result is that G>>1 within the loop bandwidth, and CL(s) and $H_{classic}$ are converted to low pass form. Figures demonstrating this will be shown.

If we are interested in the noise in Q_{nout1} from Q_{n1} when Q_{n1} is a noise signal, it is given by:

Equation 5: $$\frac{Q_{nout1}}{Q_{n1}} = \frac{G_1 G_2}{1+G_1 G_2 H} = \frac{G}{1+GH} = GH_e(s)$$

Similarly, if we examine the noise from any point "y" into which we inject noise Q_{ny} into the loop, to an output node "z", where G_{yz} is the gain from point y to point z, we find:

Equation 6: $$\frac{Q_{nzcl}}{Q_{ny}} = \frac{G_{yz}}{1+G_1 G_2 H} = \frac{G_{yz}}{1+GH} = G_{yz} H_e(s)$$

With this generalized information in mind, we may now consider the PLL block diagram of Figure 2.

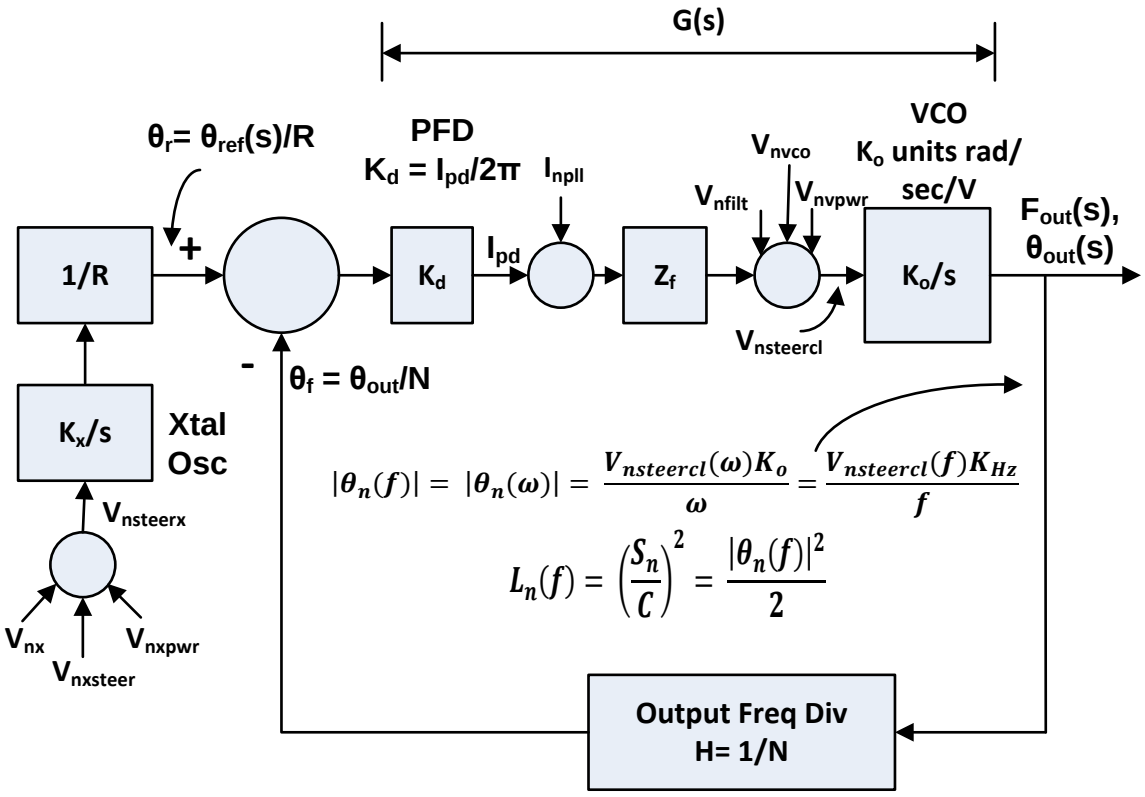

Figure 2: General PLL block diagram with noise sources. Note the phase noise equations contained in the figure for converting rms summed voltage noise V_{nsteer} to phase noise, which were derived earlier. There are so many noise sources that use of a math processing program like Mathcad or MatLab is recommended for calculations and graphs of noise terms and total noise. SPICE may also be used to build a behavioral model of the loop that provides noise.

The noise sources of this figure are:

V_{nx}: The steering input referred noise of the crystal reference oscillator, from its data sheet modified by the VCO noise modulation function and possibly by its power supply noise also.

$V_{nxsteer}$: The noise of the crystal steering input. If this source is a DAC, whose noise is often not specified, it will usually need to be stiffly RC filtered to get the induced noise well under the free running xtal floor. If a digital pot is used for the steering, it will have a predictable thermal noise, but its excess noise can be an issue. That excess current noise (Part 3 long version) will also not normally be specified by the manufacturer.

V_{nxpwr}: The input referred noise from the crystal oscillator power supply. As the reference is the heart of low noise for a modern wideband synthesizer, a low noise power supply to maintain the low noise of a high quality reference (article 3) is a good investment.

K_x: Steering gain of the crystal reference in rad/sec/V. When referring noise to the xtal oscillator input, K_x should be converted to K_{xHz}.

I_{npll}: The noise of synthesizer chip dividers and charge pump represented as a noise current. Relationships for I_{npll} based on data sheet parameters for "PLL noise" will be derived later. This representation allows easier SPICE simulation.

V_{nfilt}: The output filter voltage noise density presented to the VCO steering input.

V_{nvco}: The Leeson noise of the VCO referred to its steering input. Recall K_o is in rad/sec/V ,and when converting phase noise to an input noise voltage, K_{Hz} is used.
V_{nvpwr}: The noise effect of VCO power supply noise referred to the VCO input**.**

The error transfer function is a critical function for understanding noise transfer in the loop, as it illustrates the noise suppression inside the loop bandwidth for noise injected on a given node. For the 2nd order filter (3rd order loop), an example graph of $H_e(s)$ is shown in Figure 3. It would be pure highpass in a 2nd order loop, but here the added pole of the 2nd order filter inserts a low pass past loop bandwidth f_L.

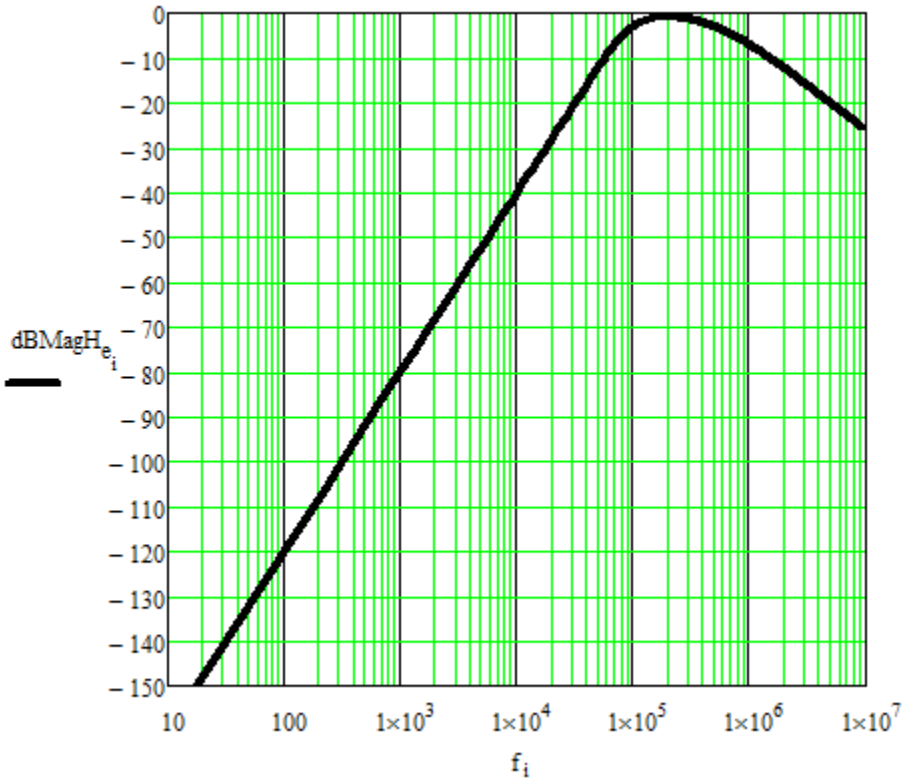

Figure 3: Error transfer function $H_e(s)$ for a 3rd order loop with f_L = 100kHz and the C_1 pole at 500kHz. For the zone of frequency from 100kHz to 500kHz there is less than 3dB noise suppression, so this tends to be where the most noise shows up. Note that inside the loop bandwidth, the noise suppression is 40dB/decade as frequency drops. This explains why the loop does such a good job of noise suppression inside its bandwidth, down to the limit allowed by synthesizer and reference noises.

The closed loop transfer function is also critical, as it illustrates the noise transfer from the crystal reference oscillator to the output. An example is shown in Figure 4.

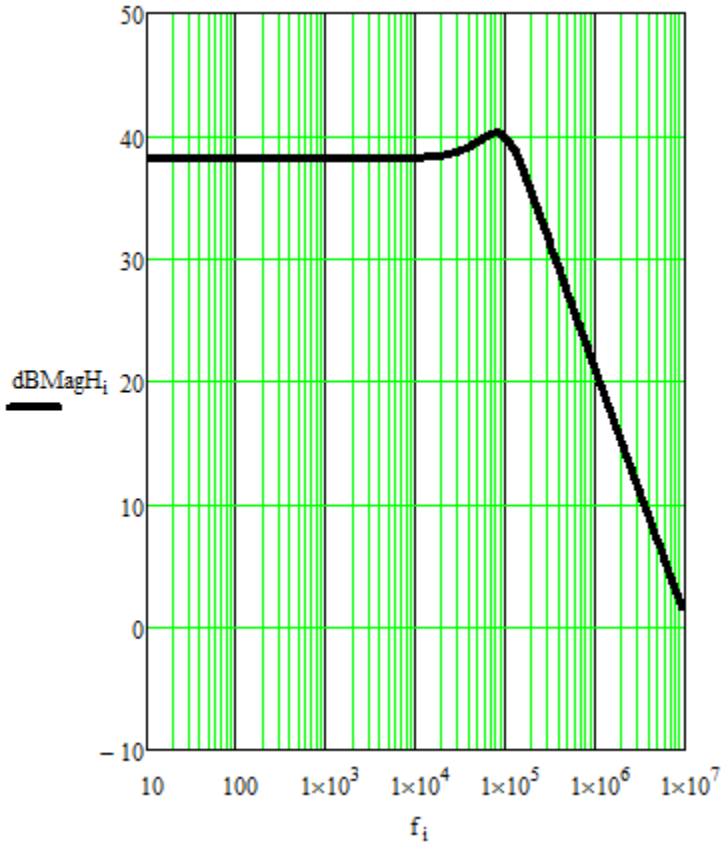

Figure 4: The closed loop transfer function from phase detector reference input to VCO output for an example case with N = 80 and loop BW f_L = 100kHz. Cascading the high pass $H_e(s)$ function with the low pass loop filter and VCO functions gives a flat response in the loop bandwidth, a few dB noise peaking around the bandwidth, and low pass past the loop bandwidth.

Note the gain in the loop bandwidth for the closed loop transfer function. This gain is the loop divide value "N", which in this example is 80. This 38dB of gain will be applied to the phase noise on the crystal reference and forced onto the VCO. Usually this multiplied crystal noise will be considerably lower than free running VCO phase noise and will be a significant improvement.

To make use of the transfer function relationships derived above for the particular PLL case, we will need the filter functions given in Table 1

Table 1: Key filter functions for embedding in transfer functions.

Filter Type & Order	**Z(f)**	**Necessary Relations**
2nd Order Passive	$Z_f(s) = \frac{1 + sT_2}{s\,A_0(1 + sT_1)} = \frac{1+sT_2}{s\,(A_1 s+A_0)}$	$A_0 = C_1 + C_2$ $A_1 = C_1 C_2 R_2$

	$= \frac{sC_2R_2 + 1}{s(sC_1C_2R_2 + C_1 + C_2)}$	$\boldsymbol{T_2 = R_2C_2}$ $T_1 = \frac{A_1}{A_0}$
3rd Order Passive	$Z_f(\boldsymbol{s}) = \frac{\boldsymbol{1 + sT_2}}{\boldsymbol{s\,A_0(1 + sT_1)(1 + sT_3)}}$ $= \frac{\boldsymbol{1 + sT_2}}{\boldsymbol{s\,A_0}(T_1T_3s^2 + (T_1 + T_3)s + 1)}$ $= \frac{\boldsymbol{1 + sC_2R_2}}{\boldsymbol{s\,(A_2\,s^2 + A_1\,s + A_0)}}$	$\mathrm{A_0 = C_1 + C_2 + C_3}$ $\mathrm{A_1 = A_0(T_1 + T_3)}$ $= \mathrm{C_2C_3R_2} + \mathrm{C_1C_2R_2} + \mathrm{C_1C_3R_3} + \mathrm{C_2C_3R_3}$ $\mathrm{A_2 = A_0T_1T_3 = C_1C_2C_3R_2R_3}$ $\mathrm{T_2 = R_2C_2}$ $T_1, T_3 = \frac{A_1 +/- \sqrt{A_1^2 - 4A_0A_2}}{2A_0}$
3rd Order Semi-Active	$Z_f(s) = \frac{G_f\,(\boldsymbol{1 + sT_2})}{\boldsymbol{s\,A_0(1 + sT_1)(1 + sT_3)}}$ $= \frac{\boldsymbol{1 + sT_2}}{\boldsymbol{s\,A_0}(T_1T_3s^2 + (T_1 + T_3)s + 1)}$ $= \frac{G_f\ (sC_2R_2 + 1)}{\boldsymbol{s\,(A_2\,s^2 + A_1\,s + A_0)}}$ $= \frac{G_f\ (sC_2R_2 + 1)}{s(sC_1C_2R_2 + C_1 + C_2)(sC_3R_3 + 1)}$	$G_f = 1 + \frac{R_{g2}}{R_{g1}}$ $\mathrm{A_0 = C_1 + C_2}$ $\mathrm{A_1 = C_1C_2}R_2 + \mathrm{C_1C_3}R_3 + \mathrm{C_2C_3}R_3$ $A_2 = C_1C_2C_3R_2R_3$ $\boldsymbol{T_2 = R_2C_2}$ $T_1 = \frac{A_1}{A_0}$ $T_3 = \frac{A_2}{A_0\,T_1}$
4th Order "Slow Slew" Active	$Z_f(\boldsymbol{s}) = \frac{\boldsymbol{1 + sT_2}}{\boldsymbol{s\,A_0(1 + sT_1)(1 + sT_3)(1 + sT_4)}}$	$\mathrm{A_0 = C_1 + C_2}$ $A_1 = A_0(T_1 + T_3 + T_4)$

R_3, C_3 are in front of the op amp, and generate the 2nd lowest frequency pole. R_4, C_4 are after the op amp, and generate the lowest frequency pole.	$= \frac{\mathbf{1} + \boldsymbol{sT_2}}{\boldsymbol{s}\,(\boldsymbol{A_3 s^3} + \boldsymbol{A_2}\,\boldsymbol{s^2} + \boldsymbol{A_1}\,\boldsymbol{s} + \boldsymbol{A_0})}$	$A_2 = A_0(T_1T_3 + T_4T_1 + T_4T_3)$ $A_3 = A_0(T_1T_3T_4)$ $T_1 = \frac{C_1C_2R_2}{A_0}$ $\boldsymbol{T_2 = R_2C_2}$ $\boldsymbol{T_3 = R_3C_3}$ $\boldsymbol{T_4 = R_4C_4}$

With a particular filter designed and with noise sources identified, we have what we need to find the closed loop noise. For the PLL block diagram with noise sources as given we may write:

Equation 7: $$\boldsymbol{G = K_d Z_f \frac{K_o}{s} = \frac{I_{pd}}{2\pi}\frac{K_o}{s} Z_f}$$

The error transfer function is used to scale noise from different points to the output. The voltage noise or noise sideband to carrier (depending on whether the output node has variable in volts or in rad/sec) generated by noise "x" at point "y" is given by:

Equation 8: $$\boldsymbol{Q_{yz} = G_{yz} H_e = \frac{G_{yz}}{1+GH} = \frac{G_{yz}}{1+\frac{I_{pd}\ K_o}{2\pi N\ \ s} Z_f}}$$

Now, we may use this relationship with the input noises to generate the rms sum of closed loop noises on the VCO input, and then the VCO noise modulation function to give the closed loop phase noise on the output.

From the rms sum of noises on the crystal oscillator tune input, we get an open loop phase noise on the crystal output θ_{nref}. This is divided by "R" and summed into the loop at the phase detector. The closed loop phase noise at the (imaginary) node following feedback phase summing is $\theta_{nrefcl} = \theta_{nref} H_e$. Therefore, the reference noise at the VCO input will be:

Equation 9: $$\boldsymbol{|V_{nxcl}| = \left| V_{nsteerx} \frac{K_{xHz}}{s} \frac{1}{R}\ K_d\ Z_f\ H_e \right|}$$

In older integer N synthesizer designs, this transfer was of lesser importance due to the narrower bandwidths of the synthesizers. If a synthesizer had only 1kHz bandwidth, then this

multiplied reference noise would be filtered off above that bandwidth, and still at a frequency usually below information bearing sidebands. But, in modern sigma delta synthesizers the bandwidth is often greater than 100kHz and may overlap information bearing sidebands and even the adjacent and alternate channels of the system. So, this is a crucially important double-edged sword of a function in these modern synthesizers. On the positive side, this noise is usually well below the phase noise of a discrete VCO and greatly below the phase noise of an integrated VCO, so the noise suppression of the loop down to approaching this multiplied crystal noise is a great benefit. On the negative side, it is a limit that requires high performance and therefore cost from the reference oscillator. Fortunately, the crystal oscillator industry is responding positively to the challenge (Part 4).

The noise from the charge pump and dividers of the synthesizer chip (often called "PLL noise") is normally handled directly at the VCO output, using methods developed by Banerjee. This model has become so popular that its parameters are often given in synthesizer datasheets. These methods shall be presented later, but first we will develop the method of summing all noise sources to get total phase noise. We assume here that we have a frequency dependent current noise function i_{npll} that can be summed into the loop filter using the transfer function approach developed above. This noise current function will be derived from the Banerjee model later. Besides allowing a unified noise analysis approach, this new model is convenient for SPICE simulation. The "magnitude function" is used in the following set of equations to emphasize that these are rms noise quantities. The noise voltage at the VCO input from the charge pump and divider noise is:

Equation 10: $$\left|V_{npllcl}\right| = \left|I_{npll} Z_f H_e\right|$$

The closed loop noises for the loop filter, input referred VCO noise, and input referred VCO power supply noise, are all on the VCO input, so are simply the open loop noises multiplied by H_e:

Equation 11: $$\left|V_{nfiltcl}\right| = \left|V_{nfilt} H_e(s)\right|$$

Equation 12: $$\left|V_{nvcocl}\right| = \left|V_{nvco} H_e(s)\right|$$

Equation 13: $$\left|V_{nvpwrcl}\right| = \left|V_{nvpwr} H_e(s)\right|$$

Recall that relations for finding V_{nvco} from the free running VCO phase noise and the input referred noise for VCO power supply were previously given.

The magnitude of the total noise on the VCO steering input is given by the rms sum of the above sources:

Equation 14: $$\left|V_{nsteer}\right| = \sqrt{\left|V_{nxcl}\right|^2 + \left|V_{npllcl}\right|^2 + \left|V_{nfiltcl}\right|^2 + \left|V_{nvcocl}\right|^2 + \left|V_{nvpwrcl}\right|^2}$$

Finally, this rms summed total noise voltage on the VCO input in the closed loop state is transformed to a **total output phase noise** by:

Equation 15: $$L(f) = \left(\frac{S}{C}\right)^2 = \left(\frac{|V_{nsteer}|K_{Hz}}{\sqrt{2}\,f}\right)^2$$

Charge Pump and Divider Noise and Corner, Synthesizer IC Figure of Merit, and Modeling

This synthesizer noise is often called "PLL noise", a term avoided here as confusion could arise as to whether this is one component of many, or total PLL noise. Let us coin the term "CPD noise" to have an accurate short term.

Flat Synthesizer Noise: Banerjee (Ref. 9) seems to have been the first (Ref. 11) to analyze and quantify this important noise source to useful accuracy in a way that can be specified in synthesizer datasheets. It is not really flat with frequency, as noise suppression in the loop is increasing as the spot noise frequency under consideration comes down from loop bandwidth (the suppression goes down as frequency in the loop bandwidth goes up). But, the noise sources being suppressed (VCO, active filter, and CPD noises) as well as the multiplied crystal noise, tend to be going down as frequency increases, so the net effect may seem fairly flat with frequency.

The largest physical source of this noise is usually the charge pumps and dividers, though less than optimum filter noise can be problem as well. Over the years, as synthesizer IC's have gotten faster, the CPD noise has dropped significantly. The main source of the noise reduction appears to be simply the narrower pulse width and less timing jitter that results from faster modern synthsizer IC's. For any given pulse width with a given jitter, we can hypothesize that there will be a floor to this noise, a term proportional to the comparison frequency (number of the narrow pulses per unit of time), and a multiplication term similar to that in multiplying the crystal reference phase noise (note the jitter noise is at the phase detector input, and adds to the jitter of the crystal reference). The resulting closed loop noise due just the frequency flat part of the CPD noise is given by:

Equation 16: $$L_{flatdB}(f) = PN1HzdB + 20log|CL(f)| + 10log\left(f_{comp}\right)$$

Here "PN1Hz" is the normalized floor on a per Hz basis. It is typically given in dB, but we will have occasion to convert it to linear when adding flat and 1/f noise powers. The empirical approach supporting this equation is proven in Ref. 11, where a timing jitter analysis leads to the same results. Measuring the key term PN1Hz for a particular synthesizer IC in this equation requires using a low noise reference and low noise VCO, with sufficient loop bandwidth that in-band noise may be driven down to the floor forced by PN1Hz, before 1/f noise applies. PN1Hz is now a standard datasheet parameter.

Inside the loop bandwidth **CL(f) ~ N,** so we have:

Equation 17: $$L_{flatdB}(f) = PN1HzdB + 20logN + 10log\left(f_{comp}\right)$$

Because N = f_{out}/f_{comp}, we may write:

Equation 18: $$L_{flatdB}(f) = PN1HzdB + 20log(f_{out}) - 10log(f_{comp})$$

Since there is noise in each phase detector pulse, the reduction of 3 dB of in-band noise for each doubling of f_{comp} in the above relation may seem odd. Doubling f_{comp} is adding 3 dB to the noise contributed by the phase detector pulses. But, doubling f_{comp} also reduces N by two, which removes 6dB of noise multiplication. The net is the 3dB improvement shown.

This simple equation has powerful results for the synthesizer industry. As radio designers, we are normally given f_{out}, and by using a smaller N value we get higher f_{comp} and lower in-band phase noise. This is the method being strongly applied by semiconductor companies with modern sigma delta fractional N synthesizers, with comparison frequencies now up to 100-200MHz (article 4). This is key to allowing on-die VCO's to have effectively low noise at required phase noise offsets, which despite heroic design efforts to improve their phase noise are still significantly noisier than the best discrete VCO's (article 4). This equation is the very heart of why fully integrated synthesizers can be sufficiently low noise for the majority of modern applications.

Flicker Synthesizer Noise: The method adopted by Banerjee to model 1/f noise in the synthesizer chip is to assume in-band noise at 10kHz is dominated by flicker, and to scale that noise by output frequency relative to 1GHz and by offset relative to 10kHz. This gives:

Equation 19: $$L_{flickerdB}(f) = PN_{1-fdB} + 20log\left(\frac{f_{out}}{1E9}\right) - 10log\left(\frac{f_{off}}{1E4}\right) = PN_{1-fdB} + 20log(f_{out}) - 10log(f_{off}) - 140dB$$

The term PN_{1_f} is used by Analog Devices as a 1/f noise parameter, and is provided in their datasheets. Texas Instruments refers to this same term as $PN_{PLL\_1/f}$. These are typically provided in dB form. In the equation above the suffix "dB" is provided to make this clear.

Linear Technology uses this same basic method for specification, but they eliminate the referencing to 1GHz carrier and 10kHZ offset. They use the normalized 1/f noise term $L_{M(NORM-1/f)}$. Let us refer to this term with the simpler variable $PN_{flicker}$ when in linear form and $PN_{flickerdB}$ when in dB form. Their equation is:

Equation 20: $$L_{flickerdB}(f) = PN_{flickerdB} + 20log(f_{out}) - 10log(f_{off})$$

Comparing these two equations, it is seen that:

Equation 21: $$PN_{flickerdB} = PN_{1-fdB} - 140dB$$

Equation 22: $$PN_{flicker} = \frac{PN_{1-f}}{1E14}$$

Combining flat and 1/f Synthesizer Noise: To add flat power to flicker power to get a total synthesizer chip noise power, we need linear terms, which are:

Equation 23: $$L_{flat} = PN_{flat} = PN1Hz\,|CL(f)|^2 f_{comp}$$

Within the loop bandwidth:

Equation 24: $$L_{flat} = PN_{flat} = PN1Hz\, N^2 f_{comp}$$

Equation 25: $$L_{flicker} = PN_{flicker} \frac{f_{out}^2}{f_{off}} = \frac{PN_{1-f}}{1E14} \frac{f_{out}^2}{f_{off}}$$

The total charge pump and divider noise at f = f_{off} is given by:

Equation 26: $$L_{cpdtot} = L_{flat} + L_{flicker}$$

Assuming that the flicker corner is within loop bandwidth, normally the case with modern sigma delta synthesizers, we may set the flicker and flat noises equal to solve for corner frequency at a particular output frequency, N, and f_{comp}. When we do this and substitute N = f_{out} / f_{comp}, we get:

Equation 27: $$f_{npllcorner} = \frac{PN_{flicker} f_{comp}}{PN1Hz} = \frac{PN_{1-f}}{1E14} \frac{f_{comp}}{PN1Hz}$$

Current Noise Model: The above noises are expressed on the VCO output in the closed loop state. Synthesizer CPD noise can also be expressed as a sum of a flat and 1/f noise current injected into the loop filter in parallel with a then assumed noise free charge pump current. This form is useful for SPICE modeling of the synthesizer noise.

The analysis to find open loop i_{npll} injected into the loop filter proceeds as follows. From our previous relations:

Equation 28: $$\frac{S}{C} = \frac{V_{npllclflat} K_{Hz}}{\sqrt{2}\ f} = \sqrt{L_{flat}} = N\sqrt{PN1Hz\, f_{comp}}$$

Equation 29: $$V_{npllclflat} = \frac{\sqrt{2}\ f}{K_{Hz}}\ N\sqrt{PN1Hz\, f_{comp}}$$

In this equation, V_{npllcl} is the closed loop flat noise from the synthesizer IC on the VCO input. We may convert this to open loop V_{npll} induced by open loop i_{npll} (the desired quantity) by considering the closed loop noise suppression $V_{npllcl} = V_{npll}\, H_e$. Since we are considering frequency well inside the loop bandwidth, we may use the 2nd order loop approximation for H_e. At frequencies well inside the loop bandwidth $H_e \sim f^2 / f_n^2$. I_{npll} may be found from the approximation what well inside the loop bandwidth the filter impedance is dominated by C_2. This gives:

Equation 30: $$V_{npllflat} = \frac{f_n^2}{f} \frac{\sqrt{2}}{K_{Hz}}\ N\sqrt{PN1Hz\, f_{comp}} = \frac{i_{npll}}{2\pi f C_2}$$

Equation 31: $$i_{npllflat} = 2\pi C_2 f_n^2 \frac{\sqrt{2}}{K_{Hz}} N \sqrt{PN1Hz\, f_{comp}}$$

From the relationship for C_2 in the 2nd order PLL we get:

Equation 32: $$f_n^2 C_2 = \frac{K_{Hz} I_{pd}}{4\pi^2 N}$$

Substituting, we find the nicely logical desired relationship for open loop noise current from the phase detector and charge pump:

Equation 33: $$i_{npllflat} = \frac{\sqrt{2}\, I_{pd}}{2\pi} \sqrt{PN1Hz\, f_{comp}}$$

Injected into the loop and properly shaped, this noise will match the normal Banerjee method above the 1/f corner of the synthesizer IC. The total noise with 1/f noise added should follow the relationship:

Equation 34: $$i_{nplltot} = \frac{\sqrt{2}\, I_{pd}}{2\pi} \sqrt{PN1Hz\, f_{comp}} \sqrt{1 + \frac{f_{npllcorner}}{f}}$$

The flicker corner is where the flat noise and 1/f noise are equal. We may check the above by setting the above relationships for flat and flicker equal and solving for f_c , which yields:

Equation 35: $$f_{npllcorner} = \frac{PN_{flicker} f_{comp}}{PN1Hz} = \frac{PN_{1-f}}{1E14} \frac{f_{comp}}{PN1Hz}$$

This is the same result we had before using the standard equations for noise directly in the VCO output. Recall $PN_{flicker}$ is the flicker noise parameter used by Linear Technology, and $PN_{1\text{-}f}$ is the parameter used by Texas Instruments and Analog Devices.

Synthesizer IC Noise Figure of Merit: Note that a lower PN1Hz, a superior flat noise, will give a higher corner frequency for the same flicker noise profile. So, a higher corner does not necessarily denote a higher noise part. It may be the very low flat noise of a superior part somewhat artificially creates and draws attention to a higher corner.

The 1/f and flat noises may be combined to give a reliable figure of merit for the total synthesizer IC noise, over a desired bandwidth f_L and with a desired phase detector frequency f_{comp}, that allows comparing the noises of candidate synthesizer IC's. If the synthesizer chip noise current i_{npltot} is integrated from 1Hz to f_L, we obtain a noise power figure of merit:

Equation 36: $$IC_{nfom} = \frac{I_{pd}^2}{2\pi^2} f_{comp} \left(PN1Hz\, f_L + f_{comp}\, PN_{flicker}\, ln(f_L) \right)$$

If two chips do not allow the same I_{pd} and f_{comp} to be used, then this equation with the I_{pd} and f_{comp} for each chip gives a figure of merit for noise power, where the lowest number is superior. Any time we are comparing two IC's with the same I_{pd} and f_{comp}, the figure of merit may be simplified to:

Equation 37: $$IC_{nfom} = PN1Hz\, f_L + f_{comp}\, PN_{flicker}\, ln(f_L)$$

Optimum Loop Bandwidth Counting All Noise Sources:

The modern sigma delta high bandwidth synthesizer generally uses the maximum bandwidth possible. This takes advantage of its ability to suppress VCO noise, even that of very low noise discrete VCO's. The "maximum possible" generally means a bandwidth where the "flat" in-band noise (which will not be exactly flat) intersects the VCO free running noise at the loop bandwidth. A lower bandwidth would mean that the VCO noise at the loop bandwidth is higher than the flat in-band noise, which will look like significant noise peaking around the loop bandwidth as that noise is suppressed moving down into the loop bandwidth. A higher bandwidth will mean that the noise induced by the synthesizer IC will be higher than the VCO free running noise at the loop bandwidth. These effects are shown inFigure 5. A possible limit to reaching ideal bandwidth is sigma delta noise, which tends to peak around one half f_{comp}, and may require using a moderately lower bandwidth. However, we may use our knowledge of the noise sources to find the ideal bandwidth where the VCO plus filter noise will match the synthesizer chip induced noise. As the bandwidth and noise are functions of each other, some iteration may be needed to arrive at the best possible solution.

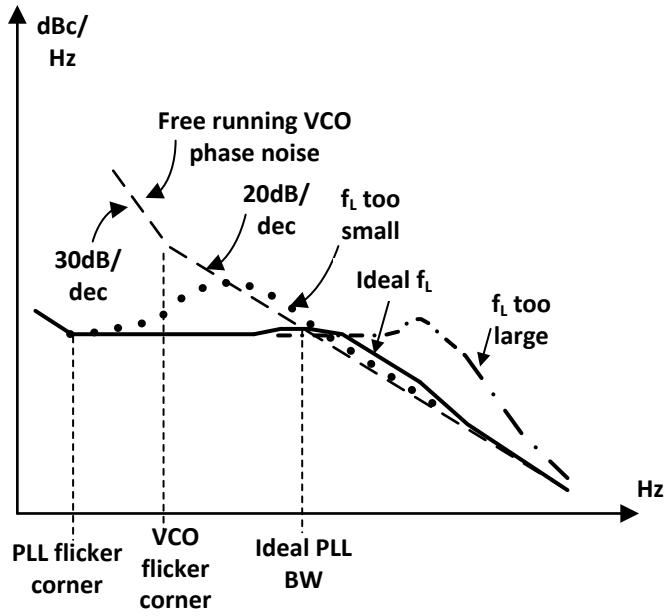

Figure 5: Illustration of ideal bandwidth vs noise effects of too small or large a bandwidth.

Ideal Passive BW for VCO Noise and Flat Synthesizer IC Noise Only: Ignoring any noise modulation of the VCO by the loop filter and the flicker corner of the synthesizer IC, we can

easily find the approximate ideal bandwidth from setting $L_{flat} = L_{VCO}$ and solving for f. This is the approach recommended by Banerjee for minimum jitter (Ref. 9, 5th edition, pp.305-306).

Assuming the desired f_L will be on the -20dB/dec part of the phase noise slope, and that we know the phase noise $L(f_{ref})$ (converted from dB), the VCO noise at a frequency f_L (the desired bandwidth) will be given by:

Equation 38: $$P_{nvco} = \quad L(f_{ref})\frac{f_{ref}^2}{f_L^2} = PN_{flat}$$

From which:

Equation 39: $$f_{L-VCO} = f_{ref}\sqrt{\frac{L(f_{ref})}{PN_{flat}}}$$

The issues we run into with this first order approximation are that we don't really get to perfectly maintain the free running VCO noise due to noise modulation by filter resistors (and op amp in the case of an active filter), and that the synthesizer IC flicker noise may not be negligible at the resulting bandwidth. We can use usually use sufficiently low power supply noise that supply noise modulation is negligible, as quite low noise integrated regulators are recently available, and if they won't do then still lower noise can be provided by discrete solutions (article 4). However, the filter noise will usually be at least noticeable and at least moderately alters the free running VCO noise. For a more accurate estimation of optimum bandwidth, these other noise sources must be taken into account.

Ideal BW with the Passive Loop Filter Including Synthesizer and VCO Flicker Noises: We get a more accurate measure of the optimum minimum jitter bandwidth when these noise sources are taken into account. These noise sources may lead to either an *increase or decrease* to that predicted using VCO noise alone. Adding loop filter noises and VCO flicker noises will push out the ideal bandwidth, because the cross over of VCO noise and the flat part of the synthesizer IC noise occurs at a higher frequency. But, counting in the higher synthesizer IC noise with synthesizer flicker tends pushes towards a lower intersection. In a particular case, either one of these may dominate. There are also noise terms from the crystal reference oscillator, but these will usually be negligible until lower offsets, as they come to dominate the locked noise on the order of 50Hz (ovenized super-low noise reference) to about 3kHz (mobile handset class VCTCXO). The crystal noise would tend to push to a lower locked bandwidth as ideal.

When we consider ideal bandwidth with the noise of a filter added to the VCO noise, in the frequency range where the bandwidth fL will fall on the -20dB/dec part of the VCO phase noise, and take account of synthesizer flicker noise, we may write:

Equation 40: $$P_{nvco} + P_{nfilt} = L_{flat} + L_{flicker} = PN1Hz\,N^2 f_{comp} + PN_{flicker}\frac{f_{out}^2}{f_L}$$

For the passive filter the noise comes from the resistors in the filter. It will be just the thermal noise as there will be no DC current in the resistors. We are mostly interested in the

noise at the loop bandwidth, where is it neither suppressed by the loop or filtered off by higher order poles. At this frequency, using the thermal noise and the VCO noise modulation function:

Equation 41: $$P_{nfilt} = \frac{M4kTR_2 K_{Hz}^2}{2f_L^2}$$

In this equation for P_{nfilt}, "M" is a multiplier for filter form. M = 1 for the first and second order filter (only R_2), M is generally about 2-3 for the third order form (adding R_3), and M is generally about 3-4 for the forth order form (adding R_3 and R_4). Now, we can get a good approximation for R_2 from the 2nd order PLL equations, where:

Equation 42: $$R_2 \cong \frac{2\pi N f_L}{K_{Hz} I_{pd}}$$

Substituting this into the equation for passive filter noise:

Equation 43: $$P_{nfilt} = \frac{M4\pi kTNK_{Hz}}{f_L I_{pd}}$$

We may substitute this relation for P_{nfilt} and the linear expressions for P_{nvco} and PN_{flat} into Equation 40, and solve for ideal bandwidth f_L. Because the expression for P_{nvco} as a function of frequency is second order, the expression for P_{nfilt} is first order, and the expression for P_{nflat} is constant, we end up with a quadratic equation:

Equation 44: $$P_{nflat} f_L^2 - \left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2 \right) f_L - L_{vco}\left(f_{ref}\right) f_{ref}^2 = 0$$

In this quadratic equation, f_{ref} is not the phase detector frequency f_{comp}, but the point on the -20dB/dec part of the VCO slope where we get an example measure of VCO phase noise. Most commonly 10kHz is used, but if the VCO flicker corner is not well below 10kHz, then a higher reference frequency should be chosen. Now, solving for ideal f_L, we of course get:

Equation 45: $$f_L = \frac{\left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2\right) \pm \sqrt{\left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2\right)^2 + 4P_{nflat} L_{vco}\left(f_{ref}\right) f_{ref}^2}}{2P_{nflat}}$$

This solution will always have a positive and negative frequency result, so there is never any doubt as to the correct root.

Note in the above that it was assumed that the final bandwidth was at a frequency greater than the VCO flicker corner. This is often but not always true. If the final bandwidth calculated using the above is in fact below the VCO flicker corner, then we must modify our design procedure. This is done by noting that for frequency f_L below the flicker corner f_{cvco} of the VCO, we have a more complicated equation for VCO free running phase noise:

Equation 46: $$P_{nvco} = L(f_{cvco})\frac{f_{cvco}^3}{f_L^3} + L(f_{ref})\frac{f_{ref}^2}{f_L^2}$$

Now when this relation for VCO phase noise is used to find f_L we get a cubic relationship that needs to be solved numerically:

Equation 47: $$P_{nflat} f_L^3 - \left(\frac{M4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2\right) f_L^2 - L_{vco}(f_{ref}) f_{ref}^2 f_L - L_{vco}(f_{cvco}) f_{cvco}^3 = 0$$

The recommended design procedure is use approximate M for the above bandwidth calculation, design the loop filter and get a better approximation for M, recalculate ideal bandwidth, and then adjust the loop filter design. If the first cut at bandwidth is near or below the VCO flicker corner, then switch to using the cubic equation for f_L. This technique rapidly converges, particularly when bandwidth and loop filter calculations are coded together in a program like Mathcad. If the calculations for filter values (article 1) and noise are coded into Mathcad, then in practice taking a few loops of adjusting part values as a function of bandwidth, noise as a function of part values, and then bandwidth as a function of noise, will rapidly lead to convergence.

Ideal Bandwidth for the Slow Slew Active Loop Filter: This inverting form loop filter is the most recommended for higher voltage tune range VCO's. For the costs of providing a low noise reference and some help converging when the op amp is not rail to rail, it provides very low noise gain and the avoidance of gain setting resistor thermal and excess noises. These resistor noises are typically dominant over the noise of the best low noise op amps, so should be avoided if possible. The only real issue to using this form is the cost and board area of a low noise reference (article 4).

An expression for the noise terms in the output of this filter was derived in the long form of article 2. Since in deriving ideal bandwidth we are concerned with the noise at the loop bandwidth, we can leave off the term for the noise of R_3. This noise is negligible at the loop bandwidth because the input pole is well above the bandwidth, the backward impedance is much greater than the forward impedance, and thus the noise gain relative to this term is <<1. Similarly, R_4 can be of such low value relative to R_2 that we can neglect its noise as well for the purpose of finding bandwidth. We will also assume that VCO supply noise has been made low enough to be negligible. Thus, the filter noises we use are:

Equation 48: $$V_{noptot}^2 = G_{n1}^2 V_{np}^2 + V_{nopR2}^2 + V_{nopInop}^2$$

Recall in the above that V_{np} is the combined op amp and reference noise. G_{n1} is the noise gain for the op amp plus input, which will usually be a small number in the range of about 1.005 to 1.02. It will be nailed down once the loop bandwidth and loop filter are fully defined. Next, we translate this noise to VCO output using the VCO noise modulation function, which gives:

Equation 49: $$P_{nfilt} = \frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2f_L^2} + \frac{4\pi kTNK_{Hz}}{I_{pd} f_L} + \frac{i_{nop}^2 2\,\pi^2 N^2}{I_{pd}^2}$$

We recall the VCO noise including noise below its flicker corner as:

Equation 50: $$P_{nvco} = L(f_{cvco})\frac{f_{cvco}^3}{f_L^3} + L(f_{ref})\frac{f_{ref}^2}{f_L^2}$$

The main equation to be used to set VCO and filter noise equal to synthesizer IC noise at the loop bandwidth f_L is:

Equation 51: $$P_{nvco} + P_{nfilt} = L_{flat} + L_{flicker} = PN1Hz\, N^2 f_{comp} + PN_{flicker}\frac{f_{out}^2}{f_L}$$

The above equations may be combined to give this equation cubic in f_L:

Equation 52: $$\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat}\right) f_L^3 + \left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - P_{nflicker} f_{out}^2\right) f_L^2 + \left(\frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2} + L_{vco}(f_{ref}) f_{ref}^2\right) f_L + L_{vco}(f_{cvco}) f_{cvco}^3 = 0$$

Here the noise gain G_{n1} from op amp plus input to op amp output at the loop bandwidth is given by:

Equation 53: $$G_{n1}^2 = \frac{V_{nopp}^2}{V_{np}^2} = \left|1 + \frac{Z_{for}}{Z_{back}}\right|^2 \cong 1$$

The expressions for Z_{for} and Z_{back} developed in the full length version of article 2 may be approximated at f_L as below.

Equation 54: $$Z_{back} = R_3 + \frac{1}{sC_3R_3} = \frac{sC_3R_3+1}{sC_3} \cong \frac{1}{j2\pi f_L C_3}\ (at\ f_L)$$

Equation 55: $$Z_{for} = \frac{1+sR_2C_2}{s(C_1+C_2+sR_2C_2C_1)} \cong R_2\ (at\ f_L)$$

Now the equation for f_L may be solved numerically using G_{n1} ~ 1.0 as an estimate, finding loop filter values using the methods in article 1, getting a more accurate estimate for G_{n1}, and iterating on circuit values and f_L until convergence. This is a quick process once a Mathcad or Excel file is built.

The above cubic relationship for f_L is to the author's knowledge the most accurate published relationship for getting an initial value for ideal loop bandwidth in the slow slew active filter case, as it takes all the major factors into account. However, it is still relying on several approximations. The most significant is the use of the 2nd order loop value for R_2. Next most significant is leaving noise from R_3 out of the calculation. After that come the approximations for Z_{for} and Z_{back} at the loop bandwidth in order to keep the calculations more tractable. These may be added for a moderate improvement in accuracy, which leads to a 4th order equation for f_L.

However, what the author recommends instead for fine tuning is to code the expressions for total resulting noise into Mathcad or Excel, and trim loop bandwidth and values for minimum noise. Mathcad has convenient non-linear equation solving and numerical integration built in, so it is preferred. This will solve several additional problems at the same time. First, it allows for eliminating the approximations above. But, it also allows for easily taking crystal reference noise and gain peaking around the loop bandwidth into account in total noise. Finally, numerically integrating for finding jitter across the bandwidth of highest interest allows minimizing the integrated noise where it matters the most, such as across an adjacent channel for best adjacent channel rejection in a communications system.

If this approach for finding absolute best loop bandwidth and parts values in the frequency offset range of greatest interest is adopted, then it may not be necessary to use the cubic equation above for finding f_L. If we ignore the VCO flicker corner on the assumption the loop bandwidth exceeds the VCO corner, then the cubic equation reduces to:

Equation 56: $$\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat}\right) f_L^2 + \left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - PN_{flicker} f_{out}^2\right) f_L + \left(\frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2} + L_{vco}\left(f_{ref}\right) f_{ref}^2\right) = 0$$

Therefore, the initial approximation for f_L becomes:

Equation 57: $$f_L = \frac{-\left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - PN_{flicker} f_{out}^2\right) \pm \sqrt{\left(\frac{4\pi kTNK_{Hz}}{I_{pd}} - PN_{flicker} f_{out}^2\right)^2 - 4\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat}\right)\left(\frac{G_{n1}^2 V_{np}^2 K_{Hz}^2}{2} + L_{vco}(f_{ref}) f_{ref}^2\right)}}{2\left(\frac{2\pi^2 i_{nop}^2 N^2}{I_{pd}^2} - P_{nflat}\right)}$$

This approximation is potentially less accurate, but if the bandwidth is adjusted via the accurate noise calculation method described above, then it can still lead to an optimum solution.

Using an ultra-low noise voltage reference and keeping resistor noise as low as possible, the slow slew inverting op amp method is the lowest noise high voltage filter method using an op amp. It may be improved still further from that presented above by using the 5th order form, where there are two input side poles, to better protect the op amp from signal bandwidths beyond its gain bandwidth product.

Ideal Bandwidth for the Semi-Active Buffered Loop Filter: This non-inverting filter form was discussed in terms of its noise in the long form of Article 2. It is shown with its noise

sources in Figure 6. Its design in terms of getting filter parts values is nearly identical to the passive filter case, simply with an additional forward gain term ($1 + R_{g2}/R_{g1}$) added in. That gain may be lumped into the VCO gain for filter part calculations.

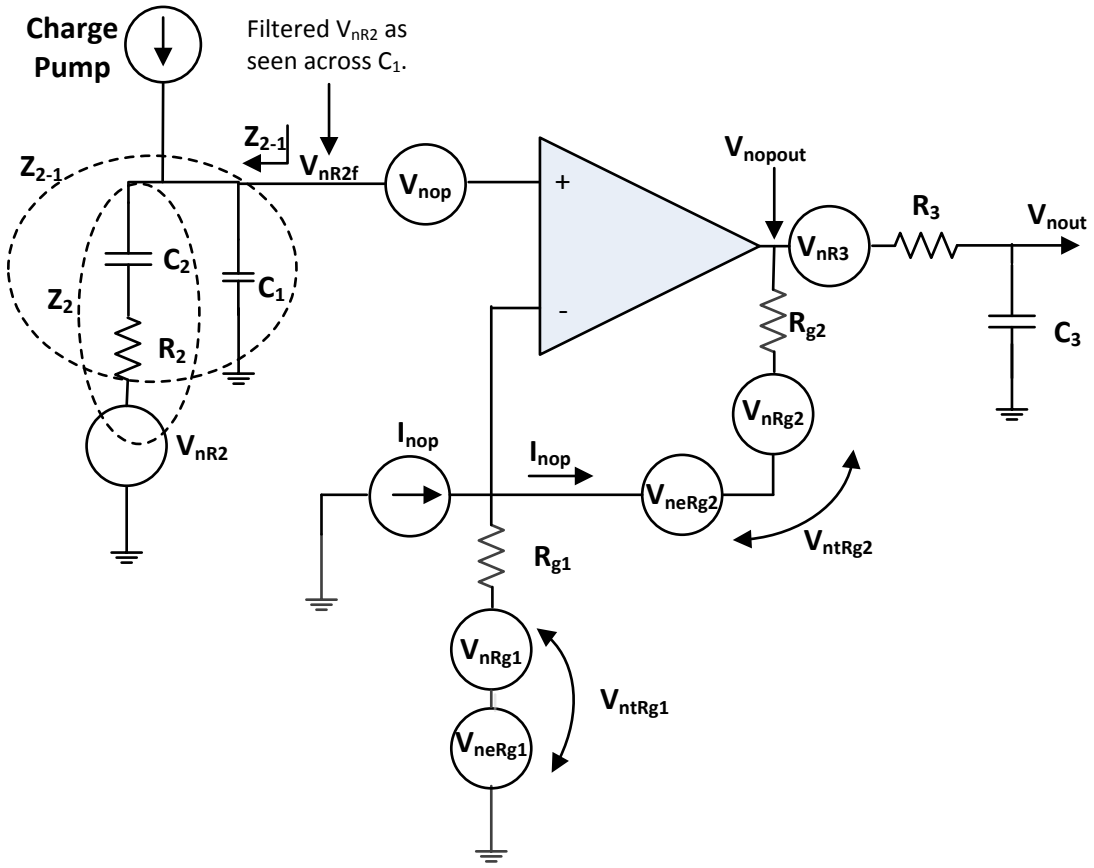

Figure 6: Buffered 3rd or 4th order semi-active filter. For 4th order, an additional RC stage is added after R_3-C_3.

It is an intuitively simple filter that allows for using VCO's whose tune range is above that of the synthesizer charge pump, and it does not require the low noise reference voltage needed by the inverting active loop filter. However, it is inferior to a well designed inverting loop filter in noise performance. It gains up the R_2 and op amp noises, has gain greater than 1 with respect to its "back" resistor noise, adds an additional noise usually greater than R_2 noise that goes straight to the output with its "forward" gain set resistor, and suffers excess noise due to current flow in the gain setting resistors. It does have one noise advantage over the inverting form, which is that the op amp noise current flows through the forward gain set resistor, and well inside the loop bandwidth this impedance is less than the C_2 impedance this noise current flows through in the inverting case. But, this larger inverting form noise well inside the loop bandwidth is suppressed by the loop action, not showing up noticeably in practice, and maintaining the advantages of the inverting form. However, despite the noise disadvantages of the non-inverting form, its attractive simplicity leads to it seeing common use, so its optimum bandwidth analysis is presented here.

The only analysis difference here are the specific noises of this filter form, including the excess current noise of the gain setting resistors that is not present in the other forms. We get a different approximate value for R_2 due to the gain of the buffer:

Equation 58: $$\boldsymbol{R_2 \cong \frac{2\pi N f_L}{G_1 K_{Hz} I_{pd}}}$$

Equation 59: $$\boldsymbol{G_1 = 1 + \frac{R_{g2}}{R_{g1}}}$$

For noise gain purposes with R_{g1} noise, we also note:

Equation 60: $$\boldsymbol{G_2 = \frac{R_{g2}}{R_{g1}}}$$

The noise at the output of the filter was previously derived as:

Equation 61: $$\mathbf{V_{noptot}^2 = \left[V_{nR2}^2 + V_{nop}^2 \right] G_1^2 + V_{nRg2}^2 + V_{neRg2}^2 + \left(V_{nRg1}^2 + V_{neRg1}^2 \right) G_2^2 + i_{nop}^2 R_{g2}^2 + V_{nR4}^2}$$

We may leave off the very low noise of R_4 for bandwidth derivation. Note in the above that the terms with "V_{ne}" are resistor excess noises. Excess spot noise voltage density V_{ne} as a function of E_{nf} = NI X 1E6 was previously derived as:

Equation 62: $$\boldsymbol{V_{ne}(f) = \frac{0.659\, E_{nf}\, R\, I_{DC}}{\sqrt{f}}}$$

Putting these together with the VCO noise modulation function and sum of flat and flicker synthesizer chip noise, we get an expression for f_L as:

Equation 63: $$\boldsymbol{P_{nflat} f_L^3 - \left(\frac{4\pi kTNK_{Hz}}{G_1 I_{pd}} - P_{nflicker} f_{out}^2 \right) f_L^2 - \left(N_R K_{Hz}^2 + L_{vco}(f_{ref}) f_{ref}^2 \right) f_L - \left(0.217 E_{nf}^2 I_{DC}^2 \right) \left(R_{g2}^2 + G_2^2 R_{g1}^2 \right) K_{Hz}^2 - L_{vco}(f_{cvco}) f_{cvco}^3 = 0}$$

We obtained this cubic equation by taking VCO flicker and excess resistor noise into account. If those are neglected, then we get the quadratic:

Equation 64: $$\boldsymbol{P_{nflat} f_L^2 - \left(\frac{4\pi kTNK_{Hz}}{G_1 I_{pd}} - P_{nflicker} f_{out}^2 \right) f_L - \left(N_R K_{Hz}^2 + L_{vco}(f_{ref}) f_{ref}^2 \right) = 0}$$

The preferred design approach is to use one of the above determinations of f_L to get a starting point bandwidth, and then iteratively trim f_L and parts values to convergence. The author recommends Mathcad or a similarly capable math program for that job.

SPICE Modeling of Synthesizers and Their Noise

SPICE or similar CAD modeling is of course one of the greatest advances in electronic design, allowing for excellent results when component models are accurate. The mathematical analysis is more flexible than SPICE, but it is quite a chore to juggle all the noise sources and control system behaviors described above. In handling this mass of data, it is quite easy to make mistakes. A SPICE analysis can confirm the correctness of the mathematical analysis, and can often be more accurate. Doing both for cross checking and then having each analysis form available to take advantage of their particular strengths allows designers the best of both worlds.

However, full SPICE analysis will not normally be possible. The user of a synthesizer IC will not typically have a full macro model of the chip to allow a mixed mode analog-digital-RF simulation, and if such a model were available it would be a very slow transient simulation requiring a high resolution FFT to transform to the frequency domain for standard phase noise viewing. But, a fast running linear system model of the loop using baseband voltages to represent RF phase and frequency can be constructed that can show accurate noise as well as transient responses so long as the loop remains in phase lock mode (when the pull-out range as described in article 1 is not violated). Such a model will not show spurs, but it can display the voltage and phase noise densities to high accuracy.

In using even a linear model, the designer must beware of DC convergence issues. The operating point voltages representing phase and frequency can converge to totally unrealistic numbers. This is particularly true when using an active loop filter. Getting the simulation to run correctly requires forcing correct DC convergence. Also, though most SPICE versions will have convenient noise analysis and often macro models of key parts like op amps with noise models built in, they do not typically have convenient stand-alone 1/f noise sources. These would be easy to code into SPICE, so the lack of these useful sources has been puzzling to the author for many years, but that is the situation. Such noise sources are needed to model VCO, crystal reference, and synthesizer IC 1/f noise corners. The designer will usually have to resort to various tricks that are dependent on the particular SPICE version to get the necessary 1/f noise sources.

In the SPICE model voltage controlled current sources driving a capacitor create the integration function needed to emulate the system action of the VCO. This approach can also be used to model the crystal reference. The mathematical method for referring phase noise to the VCO input was discussed in article 2. If the current source has transfer function "B" in A/V, then the equation for getting current gain B and C as a function of K_O is:

Equation 65: $$\frac{B}{C} = K_o$$

Recall the VCO Noise Modulation Function:

Equation 66: $$\frac{S}{C} = S_c = \frac{V_n K_{Hz}}{\sqrt{2}\, f}$$

This voltage ratio is converted to *single sided* phase noise by 20log. Thus, the equation for referring single sided VCO phase noise to tune input is:

Equation 67: $$V_{nvco} = \frac{\sqrt{2}\, f \frac{S}{C}}{K_{Hz}} = \frac{\sqrt{2}\, f\, 10^{\frac{LdB(f)}{20}}}{K_{Hz}} = \frac{\sqrt{2}\, f \sqrt{L(f)}}{K_{Hz}}$$

But, a SPICE model with a current source and capacitor system VCO model will generate *double sided* noise density on that VCO/capacitor output, which is 3dB greater than the single sided density. This conversion from actual (such as filter resistor noise) or input referred (VCO and power supply noise) to double sided output noise is given by:

Equation 68: $$\frac{S_b}{C} = S_{bc} = \frac{V_n K_{Hz}}{f}$$

When used in a SPICE model, the input referred noise is the same working from either the single or doubled sided form of sideband to carrier. To keep track of the difference, we use the correct sideband to carrier conversion from that input noise to output noise. SPICE will inherently convert input noise on a current source and capacitor integrator model of a VCO to a double sided noise on the VCO/capacitor output. That output is the place to convert to single sided noise, by multiplying the output noise by 0.707.

To use SPICE noise modeling, we need to refer VCO noise to the input. Note that on the -20dB/dec part of the VCO noise slope, the input referred noise is flat. It has a 1/f (with power) character below the corner f_{c1}. To go flat above f_{c2} on the VCO output (the floor), the input referred noise voltage must actually be rising 20dB/dec above f_{c2}. The total input referred noise is given by:

Equation 69: $$V_{nvco}^2 = N_0^2 \left[\frac{f_{c1}}{f} + 1 + \left(\frac{f}{f_{c2}} \right)^2 \right]$$

Equation 70: $$V_{nvco} = N_0 \sqrt{\frac{f_{c1}}{f} + 1 + \left(\frac{f}{f_{c2}} \right)^2}$$

In the above, N_0 is the constant noise level on the input that generates the -20dB/dec part of the phase noise curve. We find this level at a reference frequency f_{ref} that is clearly on the -20dB/decade slope.

Equation 71: $$N_0 = \frac{\sqrt{2}\, f_{ref}}{K_{Hz}}\, 10^{\frac{LdB(f_{ref})}{20}}$$

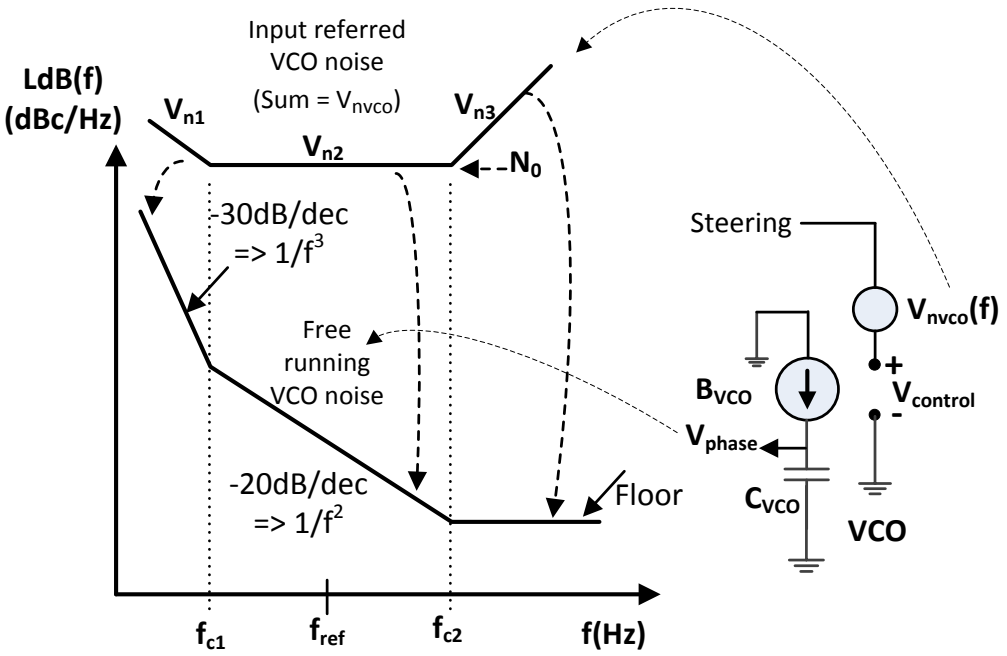

Figure 7: Shapes of VCO phase noise and input referred noise. The voltage controlled current source driving a capacitor, on the right, is how the VCO is modeled at baseband. The output voltage represents VCO phase and phase noise.

These noises are illustrated in Figure 7. We get the components of the input referred noise in a SPICE model as below.

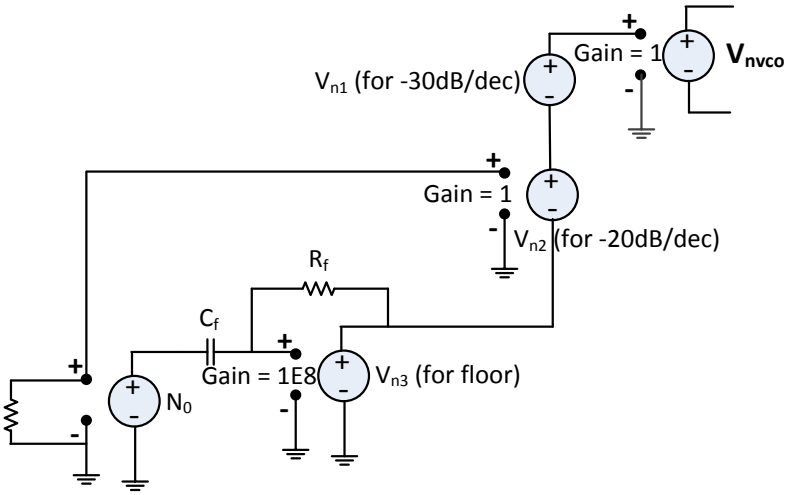

Figure 8: SPICE model for generating and summing the components of input referred VCO phase noise. The voltage noises for generating the -20dB/dec and the floor are straightforward. The component for generating -30dB/dec, the flicker component, is created by different means depending on the SPICE version. Unfortunately, most versions of SPICE do not contain a simple and generic 1/f noise source.

The noise component noise sources are given by:

Equation 72: $V_{n1} = N_0\sqrt{\frac{f_{c1}}{f}}$

Equation 73: $V_{n2} = N_0$

Equation 74: $V_{n3} = N_0\frac{f}{f_{c2}}$

The methods and equations described above are then combined into a SPICE model of the whole loop as shown in Figure 9.

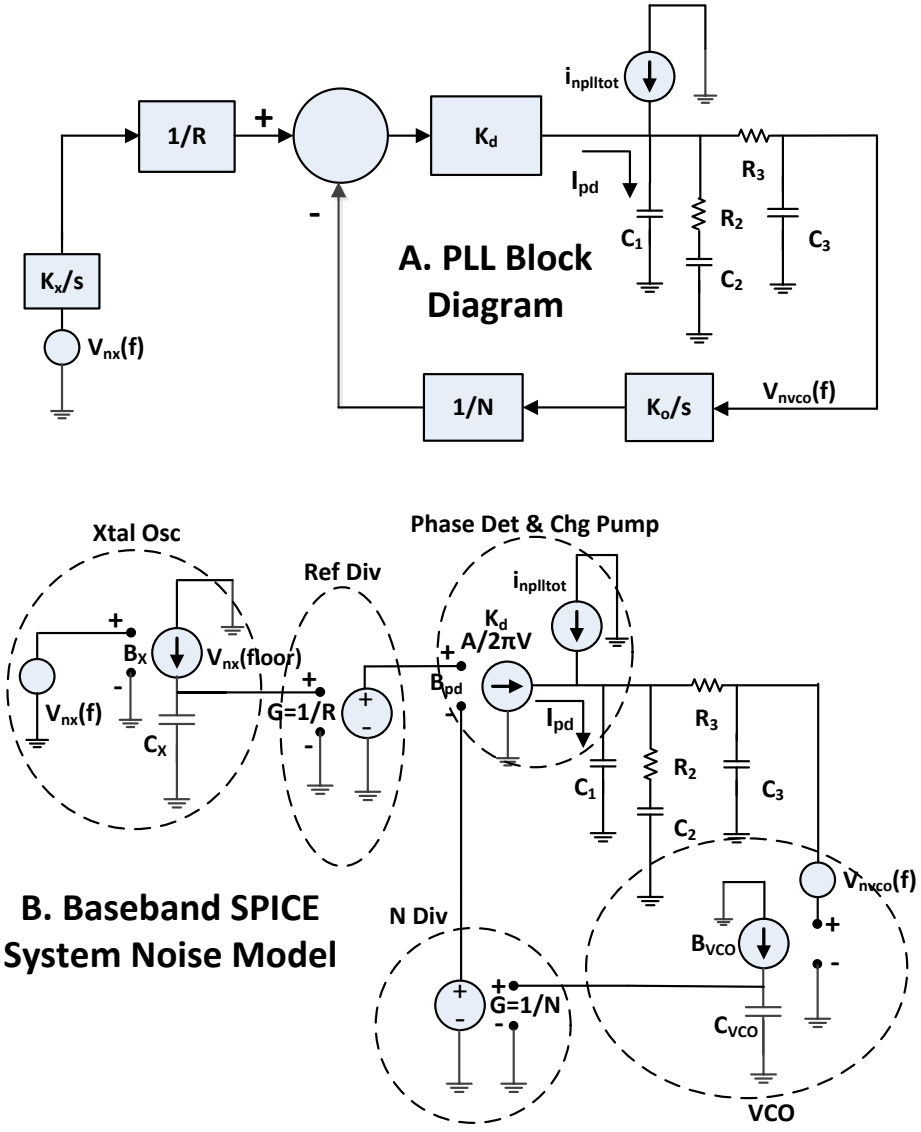

Figure 9: Block diagram of a PLL transformed into a baseband SPICE model for noise simulation. The noise current for the synthesizer chip that represents charge pump and divider

noise was derived earlier. It is modeled in SPICE similarly to the methods shown above for modeling input referred VCO noise.

Spur Noise

Spurs are discrete frequency components most commonly caused by digital noise on the phase detector output that get through the loop filter in at least noticeable form and cause modulation on the input of the VCO. These "modulated" spurs are thus symmetrical about the carrier. "Direct" spurs also exist, such as reference or clock noises that leak around the loop filter, are present in ground plane noise, or that come in through the power supply. This article will briefly review them, and refer the reader to other references (Refs 9 and 10) for more detailed coverage. Banerjee (Ref. 9) does a particularly good job in his 5th edition in covering practical prediction and control of spur noise, with chapters 16 to 21 being devoted to spurs. Egan (Ref. 10) goes deeply into the theory of fractional N synthesizer spurs as a function of modern sigma delta synthesizer architecture.

Many spur behaviors are related to the closed loop gain function of the synthesizer, given earlier as:

Equation 75: $$\frac{Q_{out}}{Q_{in}} = CL(s) = \frac{G_1 G_2}{1+G_1 G_2 H} = \frac{G}{1+GH}$$

Recall that well inside the loop bandwidth, CL(s) ~ N.

Banerjee (Ref. 9 5th edition p. 136) defines 20log of this essential function as the "Spur Gain":

Equation 76: $$\mathbf{SpurGain}\left(\mathbf{f_{spur}}\right) = \mathbf{20log}\left[\mathbf{CL}(\mathbf{j2\pi f_{spur}})\right]$$

For an integer PLL or a fractional PLL on its integer boundaries, a main spur is the "leakage spur" at the reference frequency given by (Ref. 9 3rd edition p.54):

Equation 77: $$LeakageSpur = BaseLeakageSpur + 20log\left(\frac{Leakage}{K_{pd}}\right) + SpurGain$$

This spur is caused by leakage in the charge pump current driver output, which draws charge from the loop filter capacitors which in turn has to be replaced by extra pulse width at the reference frequency. The BaseLeakageSpur is derived from small signal FM theory and is shown by Banerjee (Ref. 9 5th ed. pp. 150-151) to be approximately 16dB independent of synthesizer IC.

For fractional N PLL's, Banerjee derives theoretical tables of fractional spur amplitude (for example, 5th ed. pp.159- 165, and 3rd ed. pp. 69-79). When unfiltered spur amplitudes are known, the filtered spur amplitude is easily found from the available filter roll off:

Equation 78: $$RollOff = SpurGain - 20logN$$

This equation gives roll off as a negative dB number, so that if converted to linear it is a number less than 1 to multiply times absolute spur amplitude. Then:

Equation 79: $FilteredSpur = InbandSpur + RollOff$

Another major source of spurs that is often visible is sigma delta MASH (Multi-stAge-SHaping) spurs that occur at carrier frequency offsets around half the phase detector reference frequency (Ref. 9, 5th ed. p. 122). There can be such a large number of these spurs that they seem like a broadband noise source, sometimes seen as a "hump" of phase noise on a spectrum analyzer as displayed in some PLL analysis programs. The general solution to contain these spurs is a lower loop bandwidth and higher order loop filter. A lower sigma delta order may also help.

The delta sigma modulator order of a modern fractional N PLL is often a programmable designer choice. In general, higher order moves spurs to higher frequency, but there are trade-offs involved. Banerjee gives generalized guidance on making this choice in his 5th edition on pages 176-177. Advice on various methods to reduce or dodge spurs, such as changing VCO frequency and output divider, and optimum programming of fractional numerator and denominator, is given on pages 163-166.

Example System Phase Noise Requirements

This article series will not be taking the space to derive system requirements of multiple systems in high detail. However, as such requirements are seldom given in synthesizer text books, some approximate example requirements will be briefly derived.

Noise requirements are typically "in-channel", where phase noise competes with desired signal or modulation, or "out-channel", where phase noise may convert other signals to be on channel through the "reciprocal mixing" process. The out-channel form leads to phase noise requirements to avoid adjacent and alternate channel interference. Some systems that have multiple transmitters in close physical proximity also have both near and far out phase noise requirements for direct interference that is not sufficiently rejected by the limited skirt and ultimate floor of available filtering. Examples of such systems are cellular and land mobile base stations, and aircraft radios.

Three examples of demanding applications for low phase noise are high order QAM, land mobile radio (narrow 12.5kHz channels), cellular base stations, and land mobile radio. Modern military communications systems are often based on land mobile radio technology.

QAM Phase Noise Requirements: High order quadrature amplitude modulation (QAM) is particularly demanding on phase noise, as the QAM symbols are in a tightly packed constellation. Phase noise and power amplifier non-linearity are the two main sources that can cause a symbol point to cross the boundaries of the area of amplitude and phase assigned to each symbol. To get maximum data rate, having each symbol represent as many bits as possible is the design goal. Lower phase noise allows more bits per symbol.

From Ref. 12 we get the below table giving required integrated phase noise in degrees rms.

Table 2: Required integrated phase noise in PSK and QAM communication systems.

Bits/ Sym	Values/ Sym	Max PSK Phase Error on Local Osc	Max QAM Phase Error on Local Osc	Comments

		(deg rms)	(deg rms)	
4	16	11.3	16.9	
5	32	4.0	10.9	Interpolated
6	64	2.8	7.7	
7	128	1.8	5.2	Interpolated
8	256	0.70	3.7	
9	512	0.4	2.6	
10	1024	0.28	1.83	Extrapolated
11	2048	0.20	1.3	Extrapolated
12	4096	0.14	0.91	Extrapolated

These requirements will be considered with respect to several of the synthesizer examples given in Article 5.

Modern Cellular Base Station Phase Noise Requirements*:* The major phase noise issue in mobile communications systems is the adjacent channel and alternate channel interference specification (though "blow by" of transmitted and thus gained up phase noise in nearby receivers can also be a problem due to the limited skirts and floors of practical filters). The receive adjacent channel interference problem happens because phase noise on a receiver local oscillator that is offset one channel spacing from the center frequency will act as an LO itself, and convert adjacent channel signals to be on-channel. In radio this general process is referred to as *reciprocal mixing*. In cellular these adjacent channel signals are generally system controlled to not drastically exceed the desired signal, but they may still exceed it by several tens of dB. Thus phase noise in the offset range of channel spacing is important.

Early narrowband cellular systems have given way to much larger channel spacings using more advanced digital communications. Channel spacings are now typically 1.4 to 20MHz, so that the zone of adjacent channel interest varies from about 700kHz to 2.1MHz to as much as 10MHz to 30MHz. In these complicated systems there are a wide variety of adjacent channel interference specifications. At the base station these can vary from as little as 44dB to as much as 117dB (Ref. 14).

While the modern cellular blocking requirements are a complicated set, about 80% of such requirements are between 44dB and 86dB. It will be found in article 5 that while integrated VCO synthesizers can meet many of these, a larger set of them are met by discrete VCO synthesizers. This is due to the fact that in modern cellular the noise integration range of interest generally starts above the PLL bandwidth, where the best discrete VCO's have an advantage both on their slope and on their final floors.

The strength of an interfering signal in a nearby channel that is mixed back on channel relative to a desired signal on channel is given by the ratio of the phase noise power in the interfering channel to the local oscillator power that converts the desired signal to the IF frequency. The reciprocal blocking achieved (ratio of undesired signal power to desired signal power while still allowing successful commuications) is reduced by the required signal to noise ratio, the ratio of the desired signal power to noise or an interfering signal. Thus, the reciprocal blocking R_B from interfering sources in the band f_2 to f_3 is approximately given by:

Equation 80: $$R_B \cong \frac{1}{ReqSNR \int_{f_2}^{f_3} L(f)df}$$

This is a large number giving positive dB's when placed in decibel form. For practical low noise synthesizers it will range from about 65 to 85 dB. This result is about 2-3dB conservative since the integrated phase noise will actually spread the converted signal over about 2 channel bandwidths.

To integrate the phase noise profile to get the phase noise power from f_2 to f_3, we first need the phase noise power in convenient form we can take from a phase noise graph. On the 20dB part of the phase noise slope (where we will be for wide band systems), given L(f) at a test point f_1, the phase noise density at other frequency points on the -20dB/dec part of the phase slope is given by:

Equation 81: $$\boldsymbol{L(f) = \frac{f_1^2\, L(f_1)}{f^2}}$$

Now integrating over f_2 to f_3, we get:

Equation 82: $$\boldsymbol{\int_{f_2}^{f_3} L(f)df = f_1^2\, L(f_1)\left(\frac{1}{f_2} - \frac{1}{f_3}\right)}$$

If the interfering channel of interest reaches to the floor of the phase noise curve at frequency f_4, then we set f_2 to the floor corner and integrate the flat floor from f_3 to f_4. Naturally the relation to get the floor power is:

Equation 83: $$\boldsymbol{\int_{f_2}^{f_3} L(f)df = L(floor)[f_4 - f_3]}$$

Sometimes we need to perform this integration using one or both of the above equations, and other times it may be taken from a CAD program output being used to design the PLL and gets its noise. Often these programs give phase noise over a frequency range in terms of degrees rms. If this number is available, then we may use the above phase noise equations to find:

Equation 84: $$\boldsymbol{\int_{f_2}^{f_3} L(f)df = (1.523E-4)[\varphi_{rms}(deg)]^2}$$

Sometimes the integrated power in degrees is below the numerical floor of the CAD program, in which case we are back to using the formulas or integrating numerically in a math program.

The above relations allow seeing if a synthesizer can achieve a desired adjacent channel interference, which is often the position designers are in. We also solve for required integrated noise:

Equation 85: $$\boldsymbol{\int_{f_2}^{f_3} L(f)df \cong \frac{1}{ReqSNR\, R_B}}$$

Then the required integrated noise in degrees rms from our synthesizer CAD program to achieve the desired reciprocal blocking is:

Equation 86: $$\varphi_{rms}(deg) = 81.0\sqrt{\int_{f_2}^{f_3} L(f)df}$$

These relations will be used in article 4 to give approximate blocking performance of several synthesizer examples.

Land Mobile Radio Phase Noise Requirements: Land mobile radio is the service used by many public service and government organizations such as police, fire, and forestry. Many of its principles and methods are reused in military radio equipment. It remains popular for high reliability and emergency communications, where the cost of providing higher levels of reliability are justified due to the sometimes life critical nature of this kind of communications.

Land mobile is the technical ancestor of modern cellular, and is currently in a technical state similar to second generation cellular (first generation digital cellular). Rather than resort to the wide channel bandwidths and complicated system design of modern cellular, it keeps narrow channels and simpler design. Though it started with analog FM and 50kHz channel spacing, it is now chiefly quantized digital voice with channel spacings of 12.5kHz and 25kHz.

The following regulatory requirements usually apply. Europe is particularly strict, and meeting their requirements will usually meet requirements in other nations.

1. For Europe, EN-300-113 section 5.1.4 requires that for a channel separation of 12.5 kHz, the transmitted adjacent channel power shall not exceed a value of 60.0 dB below the transmitter carrier power (conducted) without the need to be below 0.2 µW (-37 dBm).

This implies that integrated L(f) from 6.25kHz to 18.75kHz shall not exceed -60dBc, and to have safety margin should be no higher than -70dBc. That safety margin would typically ensure that modulation splatter into the next channel is the dominant transmitted adjacent channel power. Meeting -70dBc in turn requires an average L(f) per Hz over that frequency range of no more than **-111 dBc/Hz**.

2. EN-300-113 section 5.2.5 requires:

A. Receive adjacent channel rejection of 60dB for 12.5kHz channels.
B. Receive adjacent channel rejection of 70dB for 25kHz channels.

It was derived above that:

$$\int_{f_2}^{f_3} L(f)df \cong \frac{1}{ReqSNR\ R_B}$$

is the required integrated noise power (all non-dB terms). This formula is conservative by about 2-3dB.

Assume required SNR to be 14dB, which is 25.1. Provide for 10dB safety margin in phase noise induced adjacent channel blocking.

Then for 12.5kHz channels the desired reciprocal blocking is 70dB = 1E7. The integrated power relative to carrier is thus 3.98E-9. Per Hz over 12.5kHz this is 3.18E-13 = **-125dBc/Hz**.

25kHz channels are not the norm for land mobile radio, which is fortunate since European 25kHz channel adjacent channel requirements are extreme. For 25kHz channels the desired reciprocal blocking is 80dB = 1E8. The integrated power relative to carrier is thus 3.98E-10. Per Hz over 25kHz this is 3.18E-13 = **-138dBc/Hz**.

The European receive requirements are dominant. U.S. land mobile equipment does not have an adjacent channel blocking requirement, as in general the U.S. regulations concentrate on transmitted spectra and do not dictate receiver performance. Land mobile channel plans are described by Ref. 15.

Recall the in-band noise at the output of a divide by K outside the loop is given by:

Equation 87:

$$P_N(inband) \approx P_{n1} + 20\,log\,N + 10\,log\,F_{comp} - 20\,log\,K = -20\,log\,K$$
$$= P_{n1} + 10\,log\,N + 10\,log\,F_{out} - 20\,log\,K$$

If we double the output frequency leaving N constant and get by to the original frequency by increasing K from 1 to 2, we note that 10logfout goes up 3 dB but -20logK goes down 6 dB, for a net improvement of 3 dB. So, we get a similar improvement for in-band phase noise of 3 dB per double and divide.

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