"Design Methods of Modern Ultra-Low Noise Synthesizers"
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Introduction:

This is the full length version of the first of a four-article series on low noise synthesizer design using the latest synthesizer IC's and supporting parts. Recent years have seen major changes in the frequency synthesis art, driven by a combination of advancing RFIC design and higher frequency crystal references, that are fundamentally changing the frequency sources field. Ultra-low noise discrete VCO's, which have been the heart of low noise synthesizers for decades, now find themselves challenged by integrated VCO's on the same die as the synthesizer. The best discrete VCO's still enjoy a 20-30dB phase noise superiority over the best integrated VCO's, but IC companies are conducting an asymmetric battle to dominate the market with full integration based not on the best VCO noise, but on architectural innovations that often render free running VCO noise less important. This is achieved by putting good if not great VCO's on die with SiGe BiCMOS processes and MEMS inductor resonators, and then suppressing that fairly good noise down to a very low level via feedback.

Instead of synthesizer design using a typical strategy of the narrowest loop bandwidth that frequency change time allows in order to keep the synthesizer from degrading a high quality VCO, the strategy has often totally altered to having a high bandwidth loop that can suppress noise over a wide frequency range, down to the level enabled by recent ultra-low noise dividers and charge pumps on the IC's. For lowest total integrated noise starting from a fairly low starting frequency inside the loop bandwidth, this new strategy is superior. The older standard of a low loop bandwidth usually only yields lowest noise if spur noise is a problem, or if the starting point of the frequency noise range of interest is beyond the loop bandwidth.

When using the wide bandwidth strategy, the result is that the best integrated VCO synthesizers usually have the best noise inside the loop bandwidth, as they generally have a 4-7 dB less PLL noise (divider and charge pump noise) than the best synthesizer chips that work with external VCO's, and also benefit from higher frequency operation than the best discrete VCO's are currently providing (to be explained in article 2). The best discrete VCO synthesizers still have lower noise past the loop bandwidth, and can deliver that for lower power. See Figure 1 for a conceptual illustration. This will be expanded in article 2.

The two methods are now fighting it out for design wins based on their relative advantages and how important those advantages are in different radio systems. If discrete

VCO's are moved up in frequency while maintaining superior normalized phase noise, and had the benefit of similar divider and charge pump noise, they would have better noise in-band also, and it remains to be seen if that situation will develop. That possibility is explored in article 2.

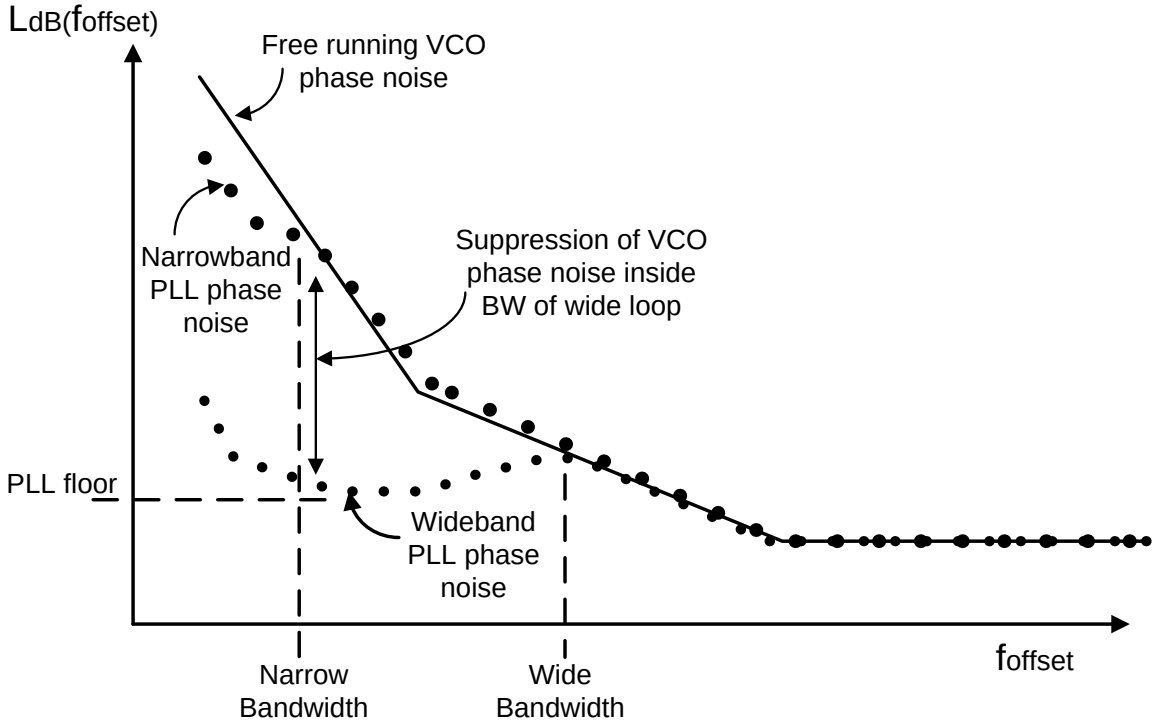

Figure 1: Suppression of noise inside the loop bandwidth has become a key technique that is altering the technology of frequency sources. When the loop bandwidth exceeds critical frequency offsets such as the distance between channels, it allows meeting key system noise specifications such as adjacent channel rejection using fully integrated VCO's.

There are many entire books devoted to frequency synthesizers, so obviously we can only cover the most important points here. It will take four articles to cover the basics of modern frequency synthesis, its design methods, and the resulting parts choices and performance results. This first article will review simple historical and modern more advanced design methods in order to set the stage. The second article will extend the modern methods to include noise and its minimization. In the noise article the methods used by modern synthesizers to allow and profit from on-die VCO's and to reduce noise to new levels will be presented, along with description of when the discrete VCO approach may be superior. The third article will review the performance and features of available subsystems and parts that go in the synthesizer system, practical noise sources to beware of, and modern software tools of PLL design. The fourth and final article will put all that together with phase noise specification methods for applications that demand the lowest noise, and practical examples of state-of-the-art low noise single loop synthesizer designs.

History:

A brief historical review helps in understanding where we are now. The age of accurate and low noise frequency sources began with the invention of the crystal oscillator in 1917 and the practical quartz crystal oscillator in 1921. The concept of using a piezoelectric rock (the quartz crystal) with its astonishingly high resonator Q and accuracy to stabilize an oscillator is one of the greatest inventions in radio, comparable to the superheterodyne receiver in its impact. World War II really saw quartz frequency control explode into high usage and impact, where it was regarded as critical to the Allied Powers (Ref. 1) as it allowed reliable narrowband communications. Quartz crystal oscillators have since become ubiquitous in modern electronics, with over 2 billion units manufactured annually, and it is no exaggeration to say that the modern communications industry could not exist without them.

However, though they are slightly tunable, quartz crystal oscillators are effectively single frequency sources. Crystal oscillators are also limited in their frequency range, with upper limits of less than 1 GHz and typical or high performance upper limits of a few hundred MHz. Until quite recently a standard frequency for high quality crystal references was 10MHz, but now 100MHz is commonly available in ovenized form and is becoming available in lower cost and power voltage controlled temperature compensated (VCTCXO) form. It will be seen how these higher reference frequencies have proven very useful in reducing synthesizer noise. See modern references 2 and 3 for detailed presentation of crystal oscillator design and performance.

To provide frequency tuning before the age of synthesizers, free running "variable frequency oscillators" (VFO's) were used. The problem with them is frequency error and drift. To contain that drift took exquisite mechanical design using heavy and expensive chassis's. Many of these products are quite beautiful physically, as much fine furniture as electronic appliances, but the cost for high performance applications was prohibitive. Long time radio amateurs will remember that a set of Collins twins (receiver and transmitter) was about half the price of a new car.

These practical limits of crystal and free running oscillators motivated the development of the PLL (phase locked loop) frequency synthesizer. The PLL synthesizer is a negative feedback control system that steers a high frequency voltage controlled oscillator (VCO) to have an output frequency that is a desired exact multiple of a reference frequency provided by a crystal oscillator (see Figure 1, which will be explained in more detail shortly). In addition to providing fine frequency stepping at virtually any frequency a VCO can provide, the PLL can suppress VCO noise inside the loop bandwidth. The PLL does this by using feedback to "transfer" the accuracy and low noise of its low frequency reference to its high frequency output, similarly to how a low noise regulator transfers the accuracy and low noise of its voltage reference to its high power output. Synthesizers can also add noise to a free running oscillator or suffer limits to how much they can suppress VCO noise with the noise of their loop filters and internal dividers and charge pumps, but it will be explained in article 2 how modern "fractional N sigma delta"

synthesizers have greatly reduced these noises. Modern PLL synthesizers are also conveniently software controlled as to operating frequency and many other parameters.

PLL's were first invented in the 1930's, but the first U.S. patent for a PLL synthesizer was not issued until 1971 (Ref. 4). Synthesizer design through the 1980's typically consisted of a discrete VCO and a set of two or more integrated circuits to perform frequency division and phase detection. The work was sufficiently new that through the 1980's and into the 1990's theses and dissertations based on what we would today consider basic techniques were still considered as academically innovative research topics (Refs. 5 and 6). The first single chip synthesizer IC's appeared in the early to mid 1990's. These still required an off-die VCO, and typically had only "integer N" dividers that stepped the VCO frequency in multiples of the divided reference frequency as provided to the phase detector. They did feature handy digital control ports and an on-die "charge pump" output that usually eliminated the need for an op amp based active loop filter and that drives phase error and thus phase detector pulse width to approach zero. The first of these the author designed with were from Fujitsu, at the time astonishing single chip devices consuming only a few mA that allowed GHz frequency sources with the luxury of firmware control. National Semiconductor soon offered pin compatible versions and excellent applications support of historical and modern significance, which will be covered here shortly.

The design methods of the 1970's to the 1990's emphasized what is called the "second order" PLL with control theory "normalized form" second order equations and loop parameters (to be explained shortly). This form is handy for easy calculations and for calculation of time domain performance like settling time. However, as early as the late 1970's (Ref. 7) higher order loops with more filter poles and accurate mathematical analyses were being promoted to better filter off digital phase detector noise terms that modulated the VCO and generated noise sidebands at multiples of the divided reference frequency. These were expanded in published work of the 1980's (Ref. 8, and Ref. 9 pp. 32-42), but were still somewhat limited in use, with the second order normalized form with sometimes an extra pole added empirically being the dominant design method. Following the publication of National Semiconductor App Note 1001 in 1996 (Ref 12) by National Semiconductor engineer Bill Keese at the beginning of the internet age with such materials easily disseminated, and the excellent modern book of his co-worker Dean Banerjee (Ref. 13) in 1998, use of higher order loop filters and theoretically sound methods to design with them appeared to become much more common. The use of such high order filters combined with precise control of loop bandwidth and phase margin will be referred to here as "modern" design.

The relentless march to higher integration and lower cost has led in recent years to full "synthesizer on a chip" IC's with integrated VCO's, generally using fractional N sigma delta (also called delta sigma) frequency synthesizers that can fine step over small fractions of the divided reference frequency. This allows a much higher reference frequency than the required tune step or channel spacing, and thus wider loop bandwidth that can suppress the rather high noise of the on-die VCO's as compared to lower noise discrete VCO's. The higher integer step and reference frequency of the sigma delta

synthesizer also allows a smaller loop frequency divider N, and thus less noise multiplication in the loop (to be explained in article 2). These improvements were needed to get better in-loop suppression of free running VCO noise, as despite excellent integrated VCO improvements they still have free running noise approximately 20 to 30 dB inferior to the best external VCO's. But, inside the loop bandwidth these IC's can offer excellent noise performance, at the cost of higher noise outside the loop bandwidth than a synthesizer using a discrete VCO module can provide. Another price to be paid is high power consumption, as getting acceptable noise in an integrated VCO generally takes much higher current than a high-Q discrete VCO. However, many modern IC's are available that allow use of lower noise off-die VCO's, and combining modern synthesizers with external VCO's can provide the lowest wideband noise of all for those applications that really demand that. An example of such an application is wide channel communications systems like modern cellular base stations, which have demanding adjacent channel performance requirements at offset frequencies typically beyond the bandwidth of the synthesizer. At these offsets the free running frequency of the VCO is key, and discrete VCO's have the advantage.

With that history in mind, we may review Figure 1 and proceed to a more theoretical understanding of PLL design and noise performance.

Basic PLL Operation and the 2nd Order Normalized Form:

Before the methods of high order design (additional filter poles to suppress noise) are presented, it is useful to review the standard second order form of PLL design that is presented in most classic text books. This form leads to quick closed form expressions for bandwidth and parts values that are useful as a starting point for higher order designs, though the capacitor of higher order forms tends to be around 2X larger to make up for the phase shift of the higher poles (allowing the zero resistor more frequency to generate phase margin). This mathematically simpler form is also more easily manipulated to develop closed form expressions for important parameters such as pull out range (the range of VCO frequency over which the PLL remains in fast settling phase lock mode and not the much slower frequency lock mode). It also allows for important noise estimates to be made. The PLL block diagram of this form is shown in Figure 2.

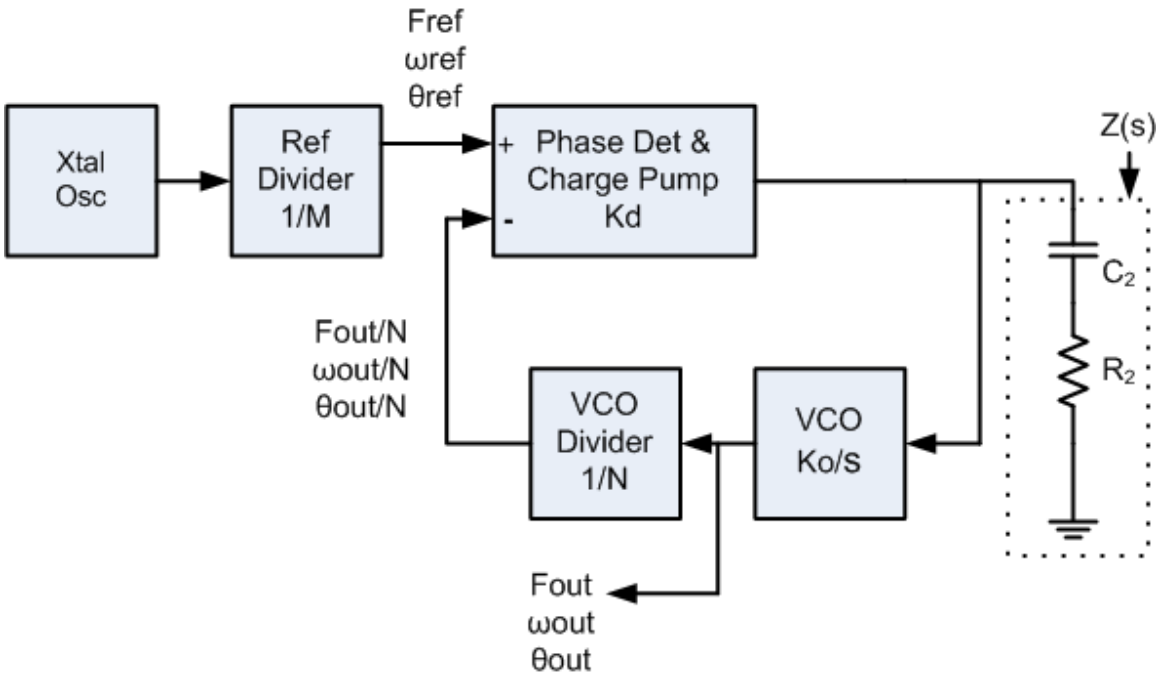

Figure 2: The classic 2nd order PLL in charge pump form**.** Units of K_o are in rad/sec/volt, and units of K_d are Id/2$\boldsymbol{\pi}$ amps/rad, where I_d is the datasheet charge pump current.

Figure 2 depicts the PLL as a feedback control system where the (divided) phase of the VCO is forced to match the (divided) phase of the crystal reference oscillator. The digital dividers are typically under firmware control, and by changing the value of the "N" divider the VCO will be forced to step in increments of the divided reference frequency. Note that while this circuit embodies digital circuits and time sampling, the sampling rate set by the reference frequency will be much higher than the loop bandwidth, and linear methods of analysis are accurate in the locked state both for part value selection and noise analysis.

The action of this feedback loop is to drive phase error to be constant or zero, which results in zero frequency error. It is a standard feedback loop with one exception that may be new to a less experienced RF engineer. We are used to thinking primarily of voltage and current as the feedback quantities, but in addition to those the PLL also treats phase and frequency as small signal frequency domain variables. When seeking lock over a wide frequency range, the modern phase/frequency detector (PFD) acts as a frequency detector to steer the VCO towards lock. When in frequency locked loop (FLL) mode, the VCO directly converts voltage input to frequency output with no feedback phase shift. Towards the end of the frequency lock mode, the loop transitions to a phase detector mode. When "phase locked" the phase detector is detecting phase as a time difference between digital edges, and driving this difference to zero. Since frequency is the time derivative of changing phase ($\omega = d\theta/dt$), phase is the integral of frequency.

Thus, in phase lock mode, the VCO acts as an integrator of input voltage to output phase. Like any integration, this introduces -90 degrees of phase shift. That is why its transfer function is in the form K_o / s, the transfer function of an integrator. K_o is here given in units of rad/sec/volt. VCO datasheets will normally give K_o in units of MHz/V. To be clear in this article series, we will refer to the Hz/V form of K_o as K_{Hz} and the radian form as K_o, so $K_o = 2\pi K_{Hz}$.

Note that with the -90 deg phase shift and the –180 degrees of negative feedback, we only have a maximum of 90 degrees of filtering phase shift allowed before -360 degrees total would result in instability. We normally leave a minimum of 40 degrees of "phase margin" at the loop bandwidth. This margin comes from the zero introduced by resistor R_2. Keeping the loop stable and with good transient response revolves around controlling the loop gain and phase margin, which is done with the loop filter design. That's why loop filter design will dominate this first article, leading to a large set of design equations covering several loop filter forms.

In the first order filter and second order PLL form the filter is the series RC circuit in shunt with the charge pump. The charge pump is a current source that is pulling or pushing current for the period of time that the two inputs of the phase detector are different. If R_2 were zero, then the charge pump driving C_2 would simple act as an integrator (the use of the subscript of "2" is in keeping with most literature, where an additional capacitor for higher order filtering in parallel with the series RC will have subscript "1"). Since this integrator would have 90 degrees of phase shift, it would use up all available phase margin and the loop would be unstable. Hence the insertion of the resistor R_2, which in transfer function terms adds a "zero", but intuitively can be viewed as preventing the full 90 degrees of loop filter phase shift that would cause instability.

In practice the 2nd order form borders on unusable with a charge pump PLL. Additional poles are usually added beyond the loop BW to provide better filtering of digital noise coming out of the phase detector (which is presenting phase error as a series of sharp edged, narrow, high frequency pulses of current), as these pulses would create strong sidebands spaced off the VCO carrier by multiples of the reference frequency. These extra poles create what is called a "high order loop", usually at least 3rd order and sometimes as high as 5th order (the loop order is one more than the filter order due to the VCO acting as an integrator). Though to the author's knowledge seldom used, there can be a need for as high as a 5th order filter and 6th order loop in the case of active loop filters, in order to not exceed op amp bandwidth limits. The filtering needed is reduced by the fact that in the charge pump form of the PLL, the width of the phase detector output pulses is forced to nearly zero since the phase error is forced to zero. The pulse width is only greater than zero as a result of noise and finite turn on and off time in the charge pump (current source) output. This very narrow width (order of one ns and as narrow as about 0.5ns) reduces the spur noise and also noise in the current output of the charge pump (if pump current is reduced to near zero, current noise in the locked state is reduced to near zero).

Now we may review basic analysis. The classic "phase transfer function" of the loop as given in older references (such as Refs 14 and 15) is defined here as:

Equation 1: $$\boldsymbol{H_{classic}(s) = \frac{\theta_{out}/N}{\theta_{ref}}}$$

$H_{classic}(s)$ is the *closed loop* transfer function from the reference input on the phase detector to the feedback input, usually referred to as simply "H(s)" in classic references. This subscript is used to clearly distinguish from the "H" that is used as part of the *open loop* transfer function in most modern literature. $H_{classic}$ will turn out to be a low pass function, and one that is highly indicative of loop locking, tracking, and noise behavior. From the figure above, if we solve for this relationship by "substituting around the loop" using the relations established in the figure, we obtain:

Equation 2:

$$\boldsymbol{H_{classic}(s) = \frac{\frac{K_o I_{pd} R}{2\pi N} s + \frac{K_o I_{pd}}{2\pi NC}}{s^2 + \frac{K_o I_{pd} R}{2\pi N} s + \frac{K_o I_{pd}}{2\pi NC}}}$$

In the above, K_o is in rad/sec/V. Note this is a low pass expression and it indicates the VCO phase and frequency will follow those of the reference out to approximately the bandwidth of the loop. Note also this is the closed loop transfer from the reference input to the phase detector to the feedback input of the phase detector. To get the transfer function from the reference input to the VCO output, we would multiply this expression by N.

This equation is in a familiar control system form where we may extract standard parameters that aid in understanding and in calculations. The standard normalized form of the second order system is given by:

Equation 3: $$\boldsymbol{H_{classic}(s) = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}}$$

The two equations are in the same form, and by equating terms we obtain the following analysis equations:

Equation 4: $$\boldsymbol{\omega_n = \sqrt{\frac{K_o I_{pd}}{2\pi NC}} = \sqrt{\frac{K_{Hz} I_{pd}}{NC}}}$$

Equation 5: $$\boldsymbol{\zeta = \frac{K_o I_{pd} R}{4\pi N \omega_n} = \frac{K_{Hz} I_{pd} R}{2N\omega_n}}$$ (ζ is the Greek letter "zeta")

The term ω_n is the "natural" frequency, and is close to but generally not equal to the open loop bandwidth. When settling, the transient response "rings down" at the natural

frequency. The term ζ is the "damping factor" and must be greater than zero for stability. Normally damping factor is set to about 0.5, which will give about 45 degrees of phase margin, or about 0.7 to 1 when an additional filtering pole is added. Phase margin is a function of both natural frequency and damping factor (this will be derived shortly). The second order normalized form of the PLL is inherently stable, as the full 360 degree phase shift around the loop to be unstable cannot be reached (the circuit architecture forces ζ > 0), but low damping factors will have a ringing settling response to frequency changes.

Again referring to Figure 2, the common PLL "error transfer function" is defined as:

Equation 6: $$\boldsymbol{H_e(s) = \frac{\theta_{ref} - (\theta_{out}/N)}{\theta_{ref}}}$$

Similar analysis shows that $H_e(s)$ may also be represented in the standard normalized form of control theory as:

Equation 7: $$\boldsymbol{H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2}}$$

$H_e(s)$ is a high pass function, whereas the phase transfer function $H_{classic}(s)$ is low pass. It is quickly shown from above that:

Equation 8: $$\boldsymbol{H_e(s) = 1 - H_{classic}(s)}$$

It will turn out that many of the modulation and noise responses of PLLs can be conveniently expressed using these functions, which is a great aid in understanding how the loop shapes noise. For example, phase or phase noise variation on the reference input to the phase detector will transfer to the VCO output proportional to the phase transfer function. Since phase transfer function is low pass, above the loop bandwidth there will be suppression of this noise or modulation. The suppression of voltage controlled oscillator phase noise inside the loop bandwidth will be according to the He(s) function given just above, down to the limits of divider noise, charge pump noise, and crystal reference noise (to be analyzed in article 2).

From the analysis equations just above we obtain the following design equations:

Equation 9: $$\boldsymbol{C_2 = \frac{K_o I_{pd}}{2\pi N \omega_n^2} = \frac{K_{Hz} I_{pd}}{N\omega_n^2}}$$

Equation 10: $$\boldsymbol{R_2 = \frac{4\pi N \omega_n \zeta}{K_o I_{pd}} = \frac{2N\omega_n\zeta}{K_{Hz} I_{pd}} \cong \frac{N\omega_L}{K_{Hz} I_{pd}}}$$

These equations are used to determine R and C based upon chosen values for natural frequency and damping factor. When extra filtering poles are introduced these values will change (particularly the capacitor), but they are still very useful starting points and serve

well for many approximations such as settling time, pull out range, and finding minimum possible thermal noise in the loop filter. The approximation for R_2 is using the approximate relationship between loop bandwidth ω_L, natural frequency ω_n, and damping factor ζ that is given later in Equation 23.

For example, a key trend is revealed above about loop filter noise that can worsen VCO noise, and how this problem has gotten much better with recent fractional N synthesizers. Note that the resistor R value is proportional to the loop divider N and inversely proportional to charge pump current Ipd. In older "integer N" synthesizers (commonly used until the early 2000's) using divided reference frequencies equal to a channel step that was typically from 12.5kHz (land mobile) to 200kHz (GSM cellular), N was a large number. For example, for GSM it was about 4500, with synthesizer chip I_{pd} of typically about 5mA, VCO gain K_{Hz} of about 20 MHz/V ($K_o = 2\pi K_{Hz}$), damping factor of 0.5, and loop bandwidth of about 20kHz. This would lead to an R value of 5.65kOhms. This resistance has a noise voltage of about 9.5nV. This is a relatively large noise voltage driving the VCO input and creating phase noise, and it limits phase noise performance to about -103 dBc per Hz at the 20kHz loop bandwidth (more technical detail on this noise will be given in article 2). This induced noise is quite a lot higher than the native VCO noise of a good quality module, which for that class of equipment in the 1990's was about -115 to -120 dBc/Hz at 20kHz offset. But, with a modern "fractional N" synthesizer that can use a high step of 100MHz and still provide 200kHz channel steps, and a charge pump of 10mA, this resistance works out to 5.65 ohms. This has a noise voltage of just 0.30nV, with the induced phase noise limit at 20kHz now hugely improved to -133 dBc per Hz. It is noteworthy that in the world of RF, where designers are fighting for every dB, that we here have an example of noise improvement in a particular source of 30dB. It illustrates that until quite recently PLL synthesizers were quite non-optimum in the area of noise. They are of course still not perfect, but huge improvements have been made.

Another very useful result that easily follows from the 2nd order form relates to the frequency range over which the PLL stays in phase lock mode and settles quickly. Best (Ref.15 p. 121) gives the pull-out range (for $\zeta < 1$) for the 2nd order digital PLL with Phase-Frequency type phase detector as:

Equation 11: $$\Delta f_{po} = N\omega_n \, exp\left[\frac{\zeta}{\sqrt{1-\zeta^2}} tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right)\right]$$

The Phase-Frequency Detector (PFD), where the phase detector has a frequency detection mode as a back-up to force lock in the case of large frequency error, is the form used in almost all modern synthesizer IC's. This allows the loop to lock even when making large frequency changes that call the phase detector to "cycle slip" when phase error exceeds the dynamic range of the phase detector (usually +/-2π). The above equation gives the frequency change *at the VCO output in Hz* that would cause the phase detector to roll over into the slower frequency lock mode. While slow, the frequency lock mode will usually converge, and as frequency comes into the pull-out range the PLL will enter phase lock mode and finish settling in a time inversely proportional to loop bandwidth.

This expression may be approximated by a curve fit as:

Equation 12: $$\Delta f_{po} = 1.838 N \omega_n (\zeta + 0.5)$$

This approximation holds for damping factor less than or greater than 1, and is still approximately true for higher order loops if a dummy damping factor appropriate to the designed phase margin is used. For phase margin of 45 degrees, a dummy damping factor of 0.5 is used in the above calculation.

When lock range is exceeded, the PLL will be in a much slower to lock frequency lock mode, from which it will after "pull in time" T_p progress to a much faster phase lock mode. Best 5th edition (Ref. 15, page 7) gives the approximate pull in time T_p to be:

Equation 13: $$T_p \approx \frac{\pi^2 \Delta\omega_{out}{}^2}{16 \zeta \omega_n^3} \approx \frac{0.1 \Delta f_{out}^2}{\zeta f_n^3}$$

In the above equation Δf_{out} is the frequency difference between the desired frequency and the starting frequency. This formula can lead to unrealistically large pull in times in the case of large changes in frequency and narrowband loops.

Introducing Modern Analysis Via the 2nd Order Form:

In modern analysis the open loop transfer function is emphasized as opposed to the closed loop 2nd order functions given above, as open loop provides direct access to the stability in the presence of more filter poles that can cause instability. Closed loop functions can also easily be found that are useful for noise transfer from various points in the loop to the VCO output. Performing modern analysis on the 2nd order form will illustrate the process, and clearly show the relationship between the past method of analysis and the now dominant modern method. It will also allow relating the loop parameters ω_n and ζ of the second order form to the open loop bandwidth ω_L and the phase margin ϕ_M of the modern form. The phase margin and loop BW will be key in designing higher order loops that can filter off phase detector spurs that the 2nd order loop would pass to the VCO input, which would in turn create noise sidebands.

Figure 3 introduces the form of feedback system modeling that will first be used in 2nd order form and then extended to higher forms.

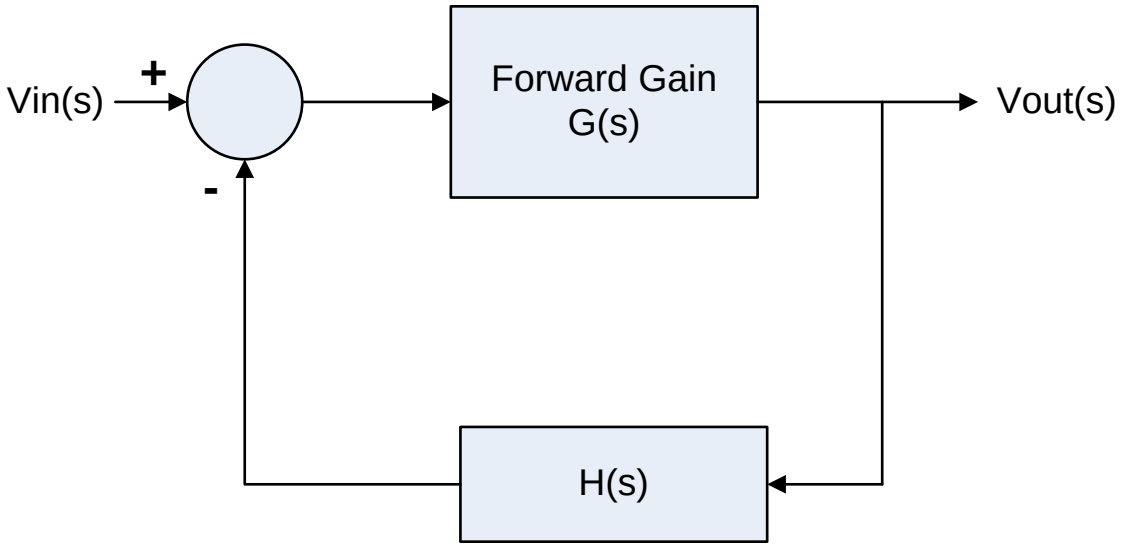

Figure 3: Simplest form of a feedback system.

Note that the feedback function is labeled "H(s)", which is in conflict with the nomenclature of the classic closed loop phase transfer function of earlier literature, but is in keeping with the modern literature. It would have been more logical to call this something like "R(s)" for reverse feedback, but the convention of calling it H(s) is now well established, so we will follow it.

We define total open loop gain as G(s)H(s). A few lines of algebra will establish the basic feedback relationship:

Equation 14: $$\frac{\mathbf{Vout}(\boldsymbol{s})}{\mathbf{Vin}(\boldsymbol{s})} = \frac{\mathbf{G}(\boldsymbol{s})}{\mathbf{1+G}(\boldsymbol{s})\mathbf{H}(\boldsymbol{s})}$$

In this equation the signals are listed as having units of voltage, but if the transfer functions apply to other variables then the same functional form can be used for any other variables. In PLLs the variables used are normally phase, frequency, voltage, and current. For example, the filter Z(s) is in units of ohms and converts an input current to an output voltage. Using Equation 14, one can define the transfer from any driving point in a feedback system to any output point, and quickly write the closed loop transfer function. When applied to PLL's, these transfer functions inevitably end up being scaled versions of either the classical phase transfer or error transfer functions.

Let us now extend this simple block diagram to a slightly more complex form to more clearly represent the PLL synthesizer.

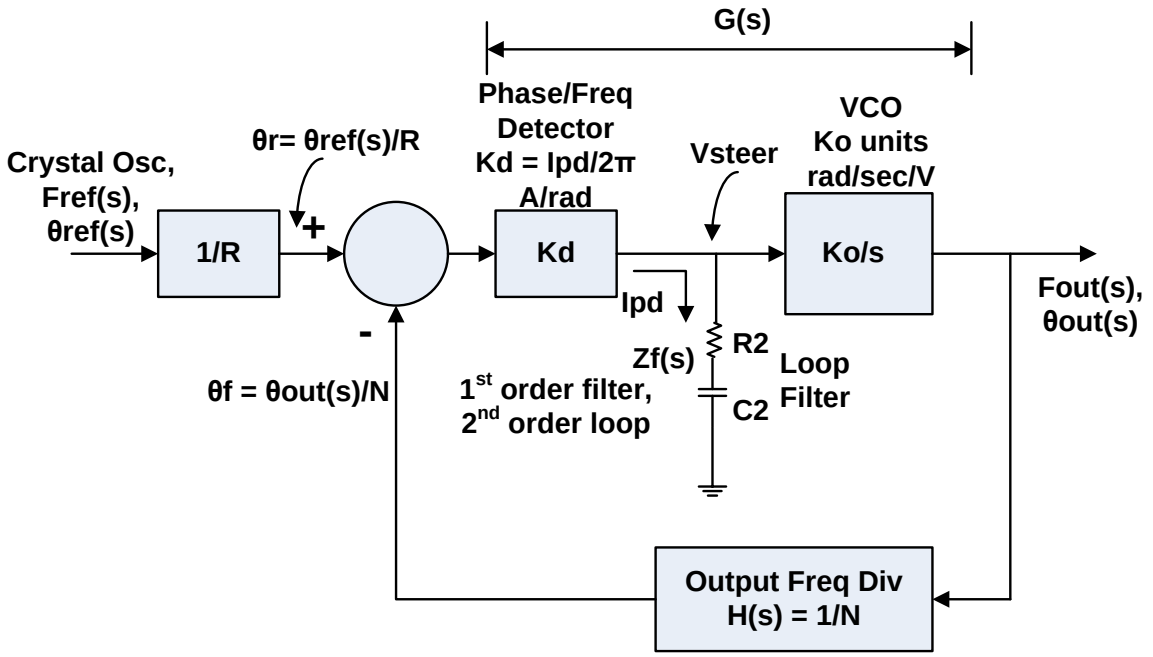

Figure 4: Simple feedback system extended to represent a 2nd order charge pump PLL synthesizer. Modern design emphasizes loop gain and phase as key parameters, and these parameters apply no matter how many poles of noise filtering are used. This figure provides a sound abstraction of PLL subsystems no matter how complicated they may internally become. Note that the 1st order filter above leads to the 2nd order PLL due to the pole in the VCO in converting voltage to phase.

In Figure 4, the forward gain G(s) is given by:

Equation 15: $$\boldsymbol{G(s) = K_d\, Z_f(s)\, \frac{K_o}{s}}$$

A note on units is again worthwhile here as we work with these transfer functions. Technically, as noted above, the units of K_d are amps per 2π radians, so this number is obtained by dividing the selected value of charge pump current by 2π. The units of K_o are rad/sec per volt, which is obtained by multiplying datasheet values of K_{Hz} by 2π. But, some authors (a key one being Banerjee) simply use the charge pump current for K_d and Hz/V for K_o. When K_d is multiplied by K_o using these datasheet units, the same numeric answer results since the factors of 2π in the numerator of K_o and denominator of K_d cancel.

The *Open Loop Gain OL(s)* is given by:

Equation 16: $$\mathbf{OL(s) = G(s)H(s) = K_d\, Z_f(s)\, \frac{K_o}{s}\frac{1}{N}}$$

This is a critical function for PLL analysis, as it captures both loop bandwidth and phase margin. Phase margin is the remaining degrees above a full 360 deg phase shift around the loop at the frequency where the loop gain (a low pass function) drops to 1.0. This frequency is referred to as *loop bandwidth* $\boldsymbol{\omega_L}$.

Since this function does not yet capture the negative inversion at the phase detector, the angle of this function adding 180 deg is the phase margin:

Equation 17: $\boldsymbol{\theta_m(\omega_L) = Ang\big(OL(s)\big) + 180deg}$

By virtue of Equation 14 above, we have the closed loop gain "CL(s)" commonly used in modern analysis from phase detector input phase to VCO output phase:

Equation 18: $\boldsymbol{CL(s) = \frac{\theta out(s)}{\theta r(s)} = \frac{G(s)}{1+G(s)H(s)}}$

When the first order filter is used as above, this is simply the 2nd order form of $H_{classic}(S)$ multiplied by N. Thus for the 2nd order loop:

Equation 19: $\boldsymbol{\frac{G(s)H(s)}{1+G(s)H(s)} = H_{classic}(s) = \frac{2\zeta\omega_n s+\omega_n{}^2}{s^2+2\zeta\omega_n s+\omega_n{}^2}}$

We may now find OL(s) of modern analysis using the 2nd order normalized parameters as:

Equation 20: $\boldsymbol{OL(s) = G(s)H(s) = \frac{2\zeta\omega_n s+\omega_n{}^2}{s^2}}$

Substituting s = jω:

Equation 21: $\boldsymbol{OL(j\omega) = \frac{\omega_n{}^2+2\zeta\omega_n j\omega}{-\omega^2}}$

We can get the phase margin as the angle of this function + 180 deg:

Equation 22: $\boldsymbol{\phi_m(\omega = \omega_L) = \tan^{-1}(\frac{2\zeta\omega_L}{\omega_n})}$

Of course, to apply this equation we need ω_L. Banerjee (Ref. 13, 3rd ed, p.119) gives this approximation, which will hold for about $\zeta > 0.4$:

Equation 23: $$\frac{\omega_L}{\omega_n} = \frac{f_L}{f_n} \cong 2\zeta$$

If we solve for the frequency where the magnitude of OL(s) = 1 (ω_L), we get a 4th order equation. However, it is quadratic in "x" after a substitution $x = \omega_L^2$. This lets us find the exact relation as:

Equation 24: $$\frac{\omega_L}{\omega_n} = \frac{f_L}{f_n} = \frac{1}{\sqrt{2}}\sqrt{4\zeta^2 + \sqrt{16\zeta^4 + 1}}$$

This equation is graphed in Figure 5, and the phase margin as a function of ζ in Figure 6. We note that $\zeta = 0.6$ corresponds to phase margin of about 56 deg.

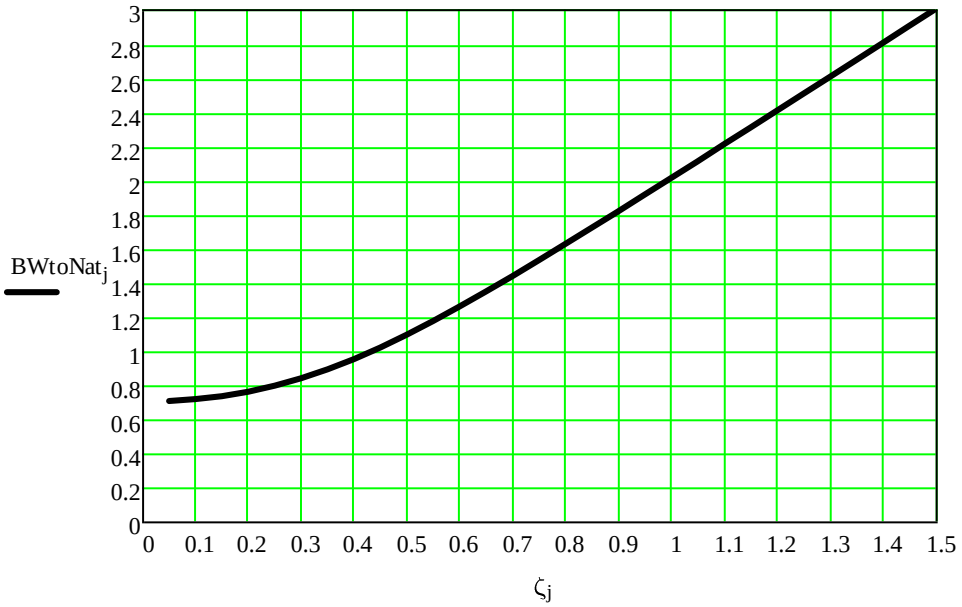

Figure 5: Ratio of 2nd order loop bandwidth to loop natural frequency as a function of damping factor ζ. The bandwidth and natural frequency are equal for $\zeta \sim 0.42$.

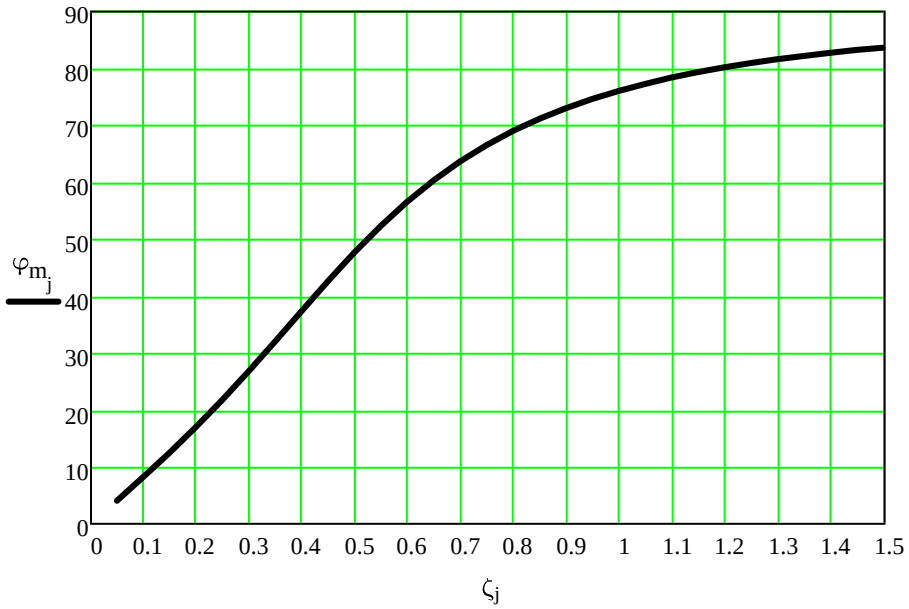

Figure 6: Phase margin as a function of ζ in the 2nd order PLL. This graph is seldom if ever given in references, and allows visualizing the available phase margin to sacrifice to higher order poles when using 2nd order analysis as a starting point. For example, if a 2nd order starting point has damping factor of 1, we see that the phase margin of 76 deg allows us to spend 21 degrees on additional filtering and still have a loop phase margin of 55 degrees.

We may also find the error transfer function in terms of the general loop subsystems above as:

Equation 25: $$\boldsymbol{H_e(S) = \frac{\theta_{ref} - \left(\frac{\theta_{out}}{N}\right)}{\theta_{ref}} = \frac{1}{1+GH}}$$

The 3rd Order Passive Filter PLL:

This form is the simplest highly usable filter and is attained simply by paralleling the series RC filter shown above with another capacitor to convert it into a 2nd order filter, as shown in Figure 7. But conceptually, this form takes us fully into modern analysis.

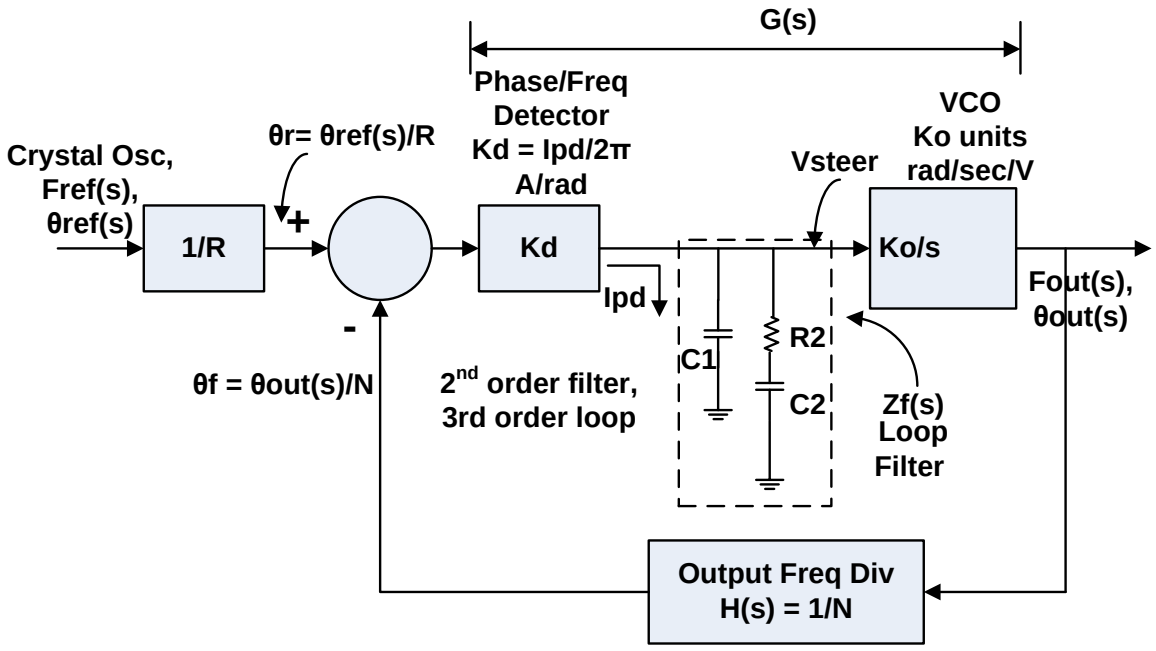

Figure 7: The 3rd order PLL is attained by adding C_1, but the implications of this simple change on loop analysis are significant.

The reason the simple addition of one capacitor has such an effect is that it fundamentally alters the phase behavior of the loop. The 2nd order loop has total phase shift approaching -360 deg at DC, but the zero introduced by R_2 brings it back from that at higher frequencies. At the loop bandwidth the phase margin is typically 40 to 70 deg, and above the loop BW phase continues rolling positive towards -270deg. But, introducing another filter pole will eventually cancel out the zero and take total phase lag back towards -360 deg.

This means that there will be a frequency where phase peaks and then declines, as shown in Figure 8.

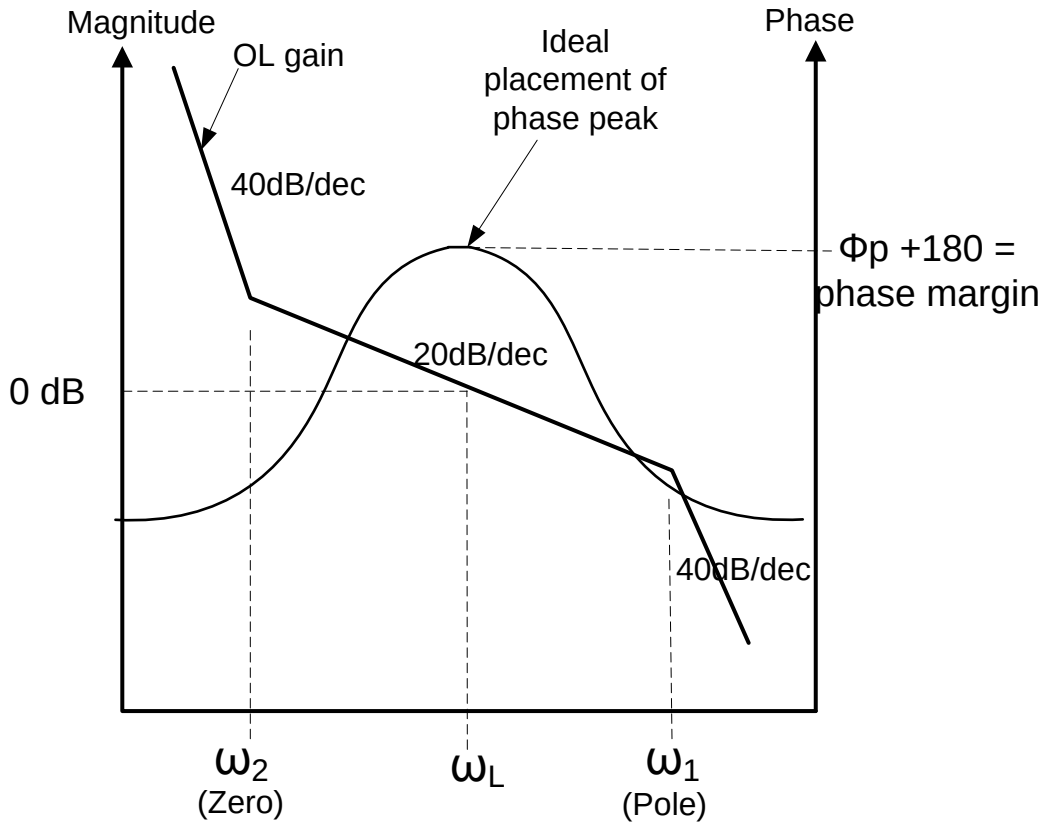

Figure 8: Open loop gain and phase in the properly designed 3rd order PLL. The maximum phase, the phase margin (when rotated 180 deg), occurs at the loop bandwidth.

We now go through the analysis of the 3rd order PLL / 2nd order filter to establish the method that will also be used for the 4th and 5th order PLL that provide even better suppression of spurs from the digital phase detection process.

The loop filter converts input current to an output voltage through its impedance, here given by:

Equation 26: $$\boldsymbol{Z(s) = \frac{1+sT_2}{s\,A_0(1+sT_1)}}$$

Here T_2 is the time constant that is the reciprocal of the zero frequency caused by R_2 working against C_2, and T_1 is the reciprocal of a pole introduced by C_1. A half page or so of circuit analysis will establish:

Equation 27: $$\boldsymbol{T_2 = R_2C_2}$$

Equation 28: $$\boldsymbol{T_1 = \frac{R_2C_2C_1}{A_0}}$$

Equation 29: $A_0 = C_1 + C_2$

The open loop gain function is given by:

Equation 30: $\mathbf{GH(s)} = \mathbf{K_d}\,\mathbf{Z_f(s)}\,\frac{\mathbf{K_o}}{\mathbf{s}}\frac{\mathbf{1}}{\mathbf{N}} = \frac{K_d K_o}{N}\,\frac{1+sT_2}{s^2A_0(1+sT_1)}$

Substituting s = jω:

Equation 31: $\mathbf{GH(j\omega)} = \frac{K_d K_o}{-N}\,\frac{1+j\omega T_2}{\omega^2 A_0(1+j\omega T_1)}$

Note in the above equation we know K_d, K_o, and N. We will choose loop bandwidth ω_L and phase margin ϕ_m. We wish to solve for A_0, T_1 and T_2, and using them and the above equations then find R_2, C_2, and C_1.

To find our three system level unknowns A_0, T_1 and T_2, we need three equations. We get them by using the above equation to find the magnitude of GH (which is 1 at ω_L), the phase of GH (which gives ϕ_m at ω_L), and the derivative of the phase of GH with respect to ω (which is zero at ω_L). This is the basic methodology for finding component values referred to here as the modern technique (as opposed to closed loop 2nd order normalized form).

The magnitude of GH is:

Equation 32: $|GH(j\omega)| = \frac{K_d K_o}{NA_0\omega^2}\,\frac{\sqrt{1+\omega^2 {T_2}^2}}{\sqrt{1+\omega^2 {T_1}^2}}$

At $\omega = \omega_L$ this magnitude is 1, and we have:

Equation 33: $A_0 = \frac{K_d K_o}{N\omega_L^2}\,\frac{\sqrt{1+\omega_L^2 {T_2}^2}}{\sqrt{1+\omega_L^2 {T_1}^2}}$

Now we're down to needing T_1 and T_2. The angle of GH is given by standard complex variable algebra. Leaving off the 180 degrees to convert from phase to phase margin we get the maximum phase margin (at ω_L) as:

Equation 34: $\phi_m = \tan^{-1}(\omega_L T_2) - \tan^{-1}(\omega_L T_1)$

The derivative of the $\tan^{-1}$ function is given by:

Equation 35: $$\frac{d(\tan^{-1} u)}{dx} = \frac{1}{1+u^2}\frac{du}{dx}$$

Applying this with general frequency ω and setting it to zero at $\omega = \omega_L$:

Equation 36: $$\frac{T_2}{1+\omega_L^2 T_2^2} - \frac{T_1}{1+\omega_L^2 T_1^2} = 0$$

Now Equation 34 and Equation 36 give us two non-linear equations in the two unknowns T_1 and T_2. We may expect we have to solve these numerically, and for higher order PLL's we will get similar equations that do have to be solved either numerically or via approximations. But, it turns out that in this particular case there is a closed form solution. Keese gives it without proof in the commonly available Ref. 12 as:

Equation 37: $$T_1 = \frac{\frac{1}{\cos\phi_m} - \tan\phi_m}{\omega_L}$$

Equation 38: $$T_2 = \frac{1}{\omega_L^2 T_1}$$

This non-obvious solution is fully derived by Rohde (Ref. 9, pp. 32-36). It takes about two pages of trigonometry and algebra to derive Equation 37, so it is not presented here. Equation 38 is easily derived in a few lines from Equation 36. One interesting consequence of Equation 38 is that the loop bandwidth is the geometric mean of the zero and the pole:

Equation 39: $$\omega_L = \sqrt{\omega_1 \omega_2}$$

We're almost done with this first look at the 3rd order loop. All that's left is to present Equation 27, Equation 28, and Equation 29 in terms of the circuit values we need. These are:

Equation 40: $$C_2 = A_0 \left(1 - \frac{T_1}{T_2}\right)$$

Equation 41: $$C_1 = A_0 - C_2$$

Equation 42: $$R_2 = \frac{T_2}{C_2}$$

The 2nd order filter and resulting 3rd order PLL are often adequate filtering of spurs for lower bandwidth loops, and is the lowest noise loop filter form for a given charge pump

current since it uses a single resistor. However, pushing bandwidth out for faster lock times and to take maximum advantage of in-band noise suppression typically requires additional poles of filtering. This is addressed next.

The 4th Order Passive Filter PLL:

This form uses the 3rd order filter shown in Figure 9. This is likely the most common filter form. If an additional stage is added to create a 4th order filter, then the entire loop is referred to as 5th order.

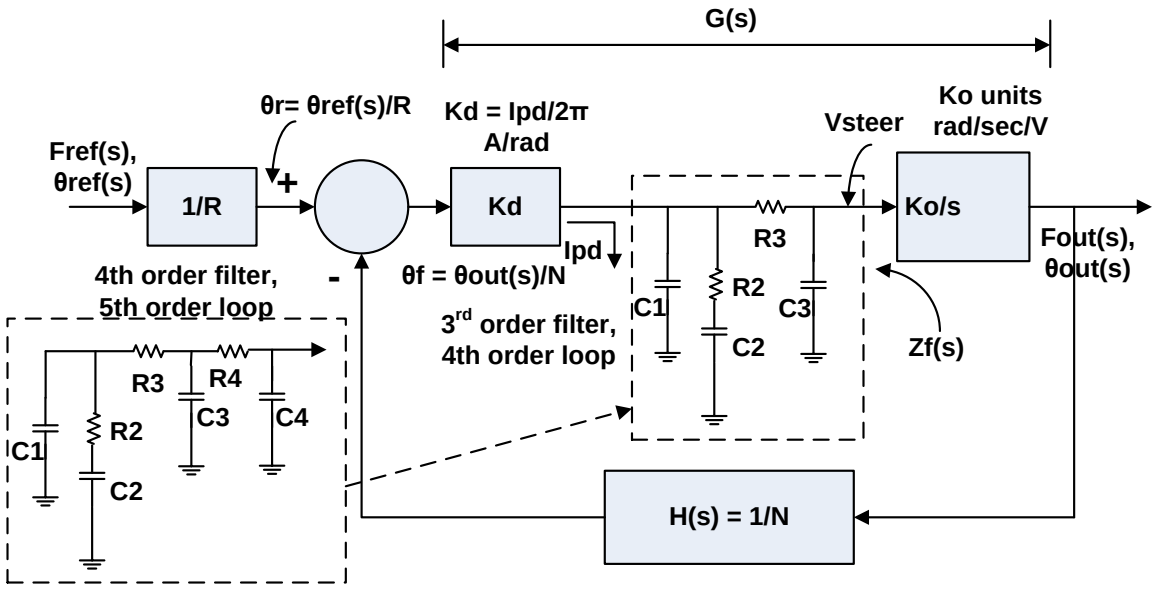

Figure 9: The 4th and 5th order PLL forms. 4th follows from 3rd by adding an RC stage, and 5th from 4th by adding another stage.

The analysis of this popular form follows the same method established for the 3rd order loop above. However, it gets more complicated (though still perfectly manageable), since the added pole introduces 2 more components but only one additional constraint. For the 5 filter components values we end up with 4 equations. Banerjee introduces the constraint to maximize C_3 using the first derivative test while still satisfying the other equations, which generates the necessary 5th equation. This has the dual benefits of suppressing the effect of VCO input capacitance and minimizing the value and thus the thermal noise of R_3. To ease analysis and provide additional flexibility Banerjee has also extended the design method with a new variable he calls the "Gamma Optimization Factor" (explained below).

Note that while we still refer to the "filter impedance", in the 3rd order filter this is not strictly the input impedance seen by the charge pump current. It is a "transfer impedance" of V_{out}/I_{in} from input current to the voltage delivered on the output of R_3, at the steering input of the VCO.

We perform the analysis similarly to the 3rd order loop. The open loop transfer function is given by:

Equation 43: $$\mathbf{GH(j\omega)} = \frac{K_d \mathrm{K_o}}{-N} \frac{1+j\omega T_2}{\omega^2 A_0 (1+j\omega T_1)(1+j\omega T_3)}$$

The filter (transfer) impedance that is part of the above is given by:

Equation 44: $$Z(s) = \frac{1+sT_2}{s\,A_0(1+sT_1)(1+sT_3)} = \frac{1+sC_2R_2}{s\left(A_2\,s^2+A_1\,s+A_0\right)}$$

We note the now familiar "zero" time constant:

Equation 45: $$T_2 = R_2C_2$$

In the above, the notation for the loop filter coefficients A_1 and A_2 is introduced, along with the familiar A_0. These coefficients are useful terms as abbreviations for lengthy functions of parts values that come from multiplying out the time constants, and are handy for solving for component values. They are given by:

Equation 46: $$A_0 = C_1 + C_2 + C_3$$

Using the magnitude function of the open loop transfer function (1 at loop BW):

Equation 47: $$A_0 = \frac{K_d \mathrm{K_o}}{N\omega_L^2} \frac{\sqrt{1+\omega_L^2 {T_2}^2}}{\sqrt{\left(1+\omega_L^2 {T_1}^2\right)\left(1+\omega_L^2 {T_3}^2\right)}}$$

We also find:

Equation 48: $$A_1 = A_0(T_1 + T_3) = C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3$$

Equation 49: $$A_2 = A_0T_1T_3 = C_1C_2C_3R_2R_3$$

We next define what Banerjee calls "pole ratios", which shall be selected by the designer based upon factors such as spur rejection. Technically these would be properly referred to as time constant ratios, but we will stay with this now standard terminology.

Equation 50: $$T_{31} = \frac{T_3}{T_1} = \frac{\omega_1}{\omega_3} = \frac{f_1}{f_3}$$

T_{31} is determining how spaced out the added pole is. A T_{31} of 1 ($\omega_3 = \omega_1$) would give the maximum spur suppression, but overlying the ω_1 pole leads to unrealizable circuit values. We must use $T_{31} < 1$. A T_{31} of 0.62 ($\omega_3 = 1.61\omega_1$) will get within 0.5dB of max spur suppression, and T_{31} of 0.5 ($\omega_3 = 2\omega_1$) will get within 1dB (Ref 13, 5th ed, p.327).

The phase margin of the open loop transfer function is given by:

Equation 51: $$\boldsymbol{\phi_m = \tan^{-1}(\omega_L T_2) - \tan^{-1}(\omega_L T_1) - \tan^{-1}(\omega_L T_{31} T_1)}$$

Applying the first derivative test to find maximum phase margin with general frequency ω, and setting this derivative to zero at $\omega = \omega_L$:

Equation 52: $$\boldsymbol{\frac{T_2}{1+\omega_L^2 T_2^2} - \frac{T_1}{1+\omega_L^2 T_1^2} - \frac{T_{31} T_1}{1+\omega_L^2 T_{31}^2 T_1^2} = 0}$$

After selecting the pole ratio T_{31}, the above two equations may be solved numerically for T_2 and T_1, thus allowing $T_3 = T_{31} T_1$.

Now we come to the "Gamma Optimization Factor". This quantity at first seems undefined other than as an approximation. Recall for the 2nd order filter and 3rd order PLL:

Equation 53: $$\boldsymbol{T_2 = \frac{1}{\omega_L^2 T_1}}$$

This may be extended in approximate form to higher order loops (Ref. 13, 5th ed, p.309):

Equation 54: $$\boldsymbol{T_2 \cong \frac{1}{\omega_L^2 (T_1 + T_3 + T_4)}}$$

For the 3rd order filter and 4th order loop considered in this section, $T_4 = 0$.

This approximation is made more accurate introducing the gamma optimization factor, where we define γ as:

Equation 55: $$\boldsymbol{T_2 = \frac{\gamma}{\omega_L^2 (T_1 + T_3 + T_4)} = \frac{\gamma}{\omega_L^2 T_1 (1 + T_{31} + T_{41})}}$$

This parameter is normally close to 1 in practical designs—in the range of 0.7 to 1.3. But, in addition to improving the accuracy of the approximation for T_2, it also indicates the behavior of the loop designed using this approximation (Ref. 13, 5th ed, p.89):

- If $\gamma = 1$, the phase peak occurs approximately at ω_L.

- If $\gamma < 1$, the phase peak occurs above ω_L.
- If $\gamma > 1$, the phase peak occurs before ω_L.

There are optimization criteria where a γ not equal to 1 has value. The 5th edition of Banerjee devotes a chapter to this subject. For example, for a T_{31} of 60% that comes within 0.5 dB of maximum spur suppression, minimum lock time occurs at phase margin of 47 deg and a gamma of 1.14 (Ref. 13, 5th ed, p.318).

Substituting Equation 55 (with T_{41}=0) into Equation 51, we get this approximation:

Equation 56: $$\boldsymbol{\phi_m = \tan^{-1}\left(\frac{\gamma}{\omega_L T_1(1+T_{31}+T_{41})}\right) - \tan^{-1}(\omega_L T_1) - \tan^{-1}(\omega_L T_{31} T_1)}$$

The above has only T_1 as an unknown. It may be solved numerically, but an approximation can be found by using $\tan^{-1}(x) \sim x$ for small x. The result is:

Equation 57: $$\boldsymbol{T_1 \cong \frac{\frac{1}{\cos\phi_m} - \tan\phi_m}{\omega_L(1+T_{31})}}$$

These two equations can be used for an approximate solution, or they can be used as starting points in the numerical solution to find exact values for T_1 and T_2.

The other two time constants follow immediately.

Equation 58: $$\boldsymbol{T_3 = T_1 T_{31}}$$

And, when using the approximate approach:

Equation 59: $$\boldsymbol{T_2 \cong \frac{\gamma}{\omega_L^2 (T_1+T_3)}}$$

We find A_1 and A_2 from:

Equation 60: $$\boldsymbol{A_1 = A_0(T_1 + T_3) = C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3}$$

Equation 61: $$\boldsymbol{A_2 = A_0T_1T_3 = C_1C_2C_3R_2R_3}$$

Recall:

Equation 62: $$\boldsymbol{T_2 = R_2C_2}$$

Now we are almost in position to pursue component values. But, we only have the four equations to get the five values C_1, C_2, C_3, R_2, and R_3. The logical method adopted by Banerjee is to find the largest C_3 that satisfies these four equations. The equations just above may be manipulated to find C_3 as a function of C_1:

Equation 63: $$C_3 = \frac{-T_2^2 C_1^2 + T_2 A_1 C_1 - A_2 A_0}{T_2^2 C_1 - A_2}$$

Applying the first derivative test for the value of C_1 that peaks C_3:

Equation 64: $$C_1(max\ C_3) = \frac{A_2}{T_2^2}\left(1 + \sqrt{1 + \frac{T_2}{A_2}(T_2 A_0 - A_1)}\right)$$

Everything needed to find this C_1 is known at this point, and it may be plugged into Equation 63 to find C_3. Then the final values are found from:

Equation 65: $$C_2 = A_0 - C_1 - C_3$$

Equation 66: $$R_2 = \frac{T_2}{C_2}$$

Equation 67: $$R_3 = \frac{A_2}{C_1 C_3 T_2}$$

Though this seems involved, it is actually a fairly simple procedure to go through once system requirements have allowed choosing the crystal reference, the VCO and thus Ko (frequency coverage and noise requirements dominate this) , the synthesizer chip and thus I_d (the max available or close to it will normally be used), the particular N or range of N to be used, ω_L, phase margin, T_{31}, and gamma (quite often there is no reason to deviate from 1.0).

Passive Filter 5th Order PLL's:

The passive 4th order filter form (see Figure 9) will be qualitatively discussed here, with the interested reader referred to Banerjee for more detail. The addition of the extra RC stage provides moderate improvement in far out spur rejection over the 3rd order filter. Speaking very approximately, the benefit of the 3rd order loop filter over the 2nd is about 2 to 7 dB, while the benefit of the 4th order filter over the 3rd is about 1-3 dB (Ref. 13, 5th ed, p.324). Realizing the few dB benefit at very high frequencies can be difficult because high frequency spurs may be crosstalk limited rather than ideal filter transfer function limited. Techniques for limiting crosstalk contamination will be presented in article 2.

However, in return for moderately better spur performance, it also introduces an additional resistor noise source in R_4. As this resistor is typically larger than R_3 due to the need to not load the preceding stage, its noise contribution is usually larger. For reasons to be presented in article 2, this noise is usually largest right around the loop bandwidth. It is case by case as to whether this additional noise is worth the far-out spur suppression.

Calculation of this case is quite involved. The 5th order PLL has 7 loop filter values to be chosen, but only 5 PLL parameters. As expected from the above, a logical constraint to apply is to maximize C_4. However, strict maximization is a complex procedure with no guarantee the rest of the parts are realizable.

Banerjee recommends an approximate method instead (Ref. 13, 5th ed., pp.353-360). This method involves an algorithm for estimating a range of viable R_3 and C_1 from the methods shown for the 3rd order filter. This simplifies the mathematics, and a candidate solution is found. If further improvement seems possible, the solution is iterated with different R_3 and C_1 in the identified range. There is no proof that solutions will always result in positive real component values, but if $T_{31} + T_{43} < 1$, then positive real values have been found in all cases tried.

Op Amp Active Filter PLL's:

Op amps used to be standard practice in PLL loop filters to convert a voltage based phase detector output to a current. Since the charge pump PLL established market dominance several decades ago, the primary reason for using an op amp has been to extend the voltage range of the loop filter to allow controlling VCO's with large tune ranges. This allows for lower K_o for any required frequency range, and for reasons that will be shown in article 2 it allows for lower induced noise on the VCO. If a designer needs to improve upon the noise of the best integrated VCO synthesizers, the op amp based loop filter with high tune range discrete VCO will often be the method.

Besides the noise benefit of low K_o, there are several additional benefits:

- The noise of modern low noise op amps extends down to approximately 1nV per root Hz. This is similar to the thermal noise in a 50 ohm resistor, so it is common for op amp noise to be a second order noise source.
- The op amp allows decoupling of resistors in the loop filter, allowing
    - Lower value resistors with lower thermal noise.
    - Placing the lowest frequency pole after the op amp where it gets maximum noise filtering effect.
    - Simplification of the analysis, even in the 4th order filter case.

There are several topologies for op amp based loop filters, but here a single preferred one will be presented (Figure 10), and given in full 4th order filter / 5th order loop form. For this filter at least the 4th order form is recommended in order to minimize the effects of limited op amp bandwidth. It may be that the optional 5th order form is needed in some cases, where an extra filter pole is used on the input side of the op amp. The single filter

pole shown will convert charge pump current pulses to small ramps, but with modern IC's these ramps are of short duration, on the order of 1ns. An additional pole would convert the ramps to longer RC exponentials that may be selected to have their main frequency content within the bandwidth of the op amp.

The basic method of component selection will be developed here using the pattern shown above, which will then be supplemented with methods based on avoiding limits of the charge pump and op amp. Detailed noise analysis methods will be shown in article 2, op amp and other component trade-offs presented in article 3, and examples in article 4.

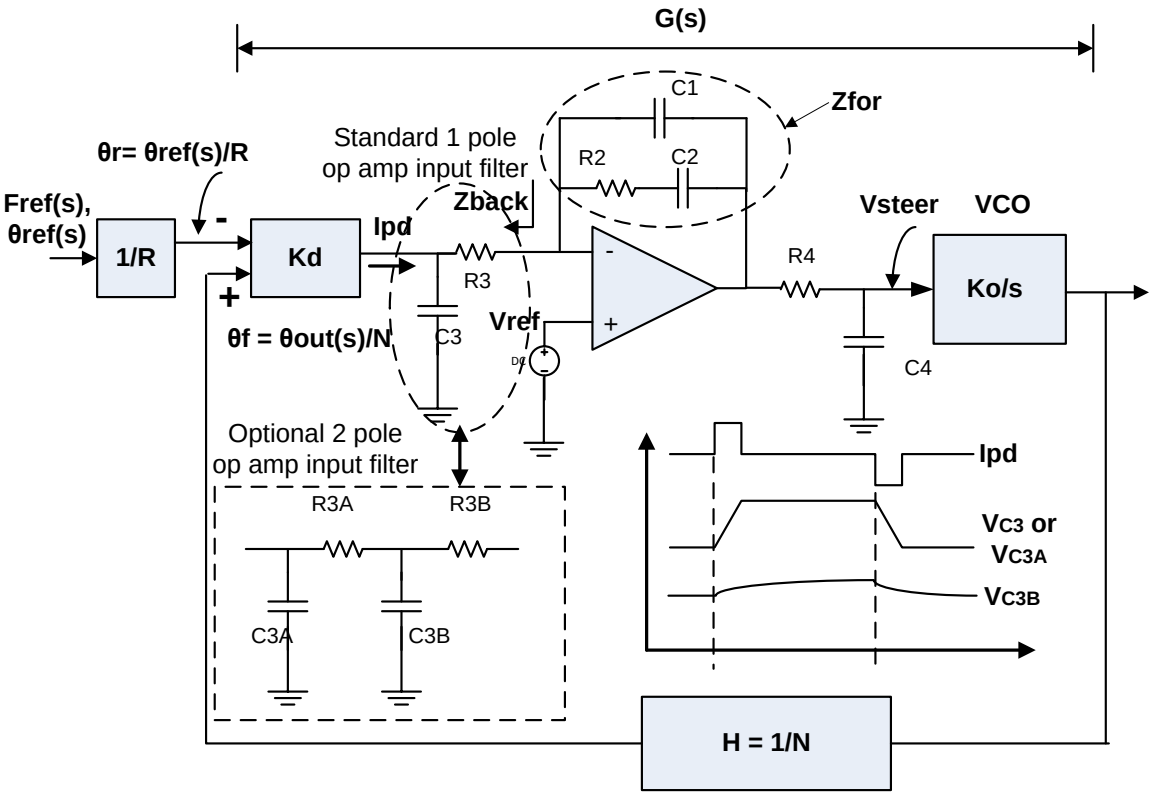

Figure 10: Active 4th order filter and 5th order PLL, with option for 5th order filter and 6th order PLL. Note that because of the inversion in the op amp, the position of the "+" and "-" on the phase detector input have been switched to keep the correct sense of negative feedback. Most synthesizers allow this to be programmed. This filter is sometimes referred to as a "slow slew rate" active filter, as the input RC reduces the slew rate and bandwidth requirements on the op amp. As it happens, C_1 also reduces the slew rate requirement, as well as suppressing spurs from the ringing response of the op amp to charge pump pulses. Slew rate requirements may be limited by judicious part value selection. Still, meeting op amp bandwidth requirements may lead to putting an additional pole ahead of the op amp, as shown with the optional 2 pole input filter.

Basic operation of this filter is as follows. A DC reference voltage is provided at the positive input of the op amp, and the combination of loop action and op amp action will be to keep the negative input of the op amp at this same voltage. This reference voltage

needs to be very low noise so as not to add noticeable noise to the loop filter (parts and methods will be covered in article 3).

The charge pump current flows into the input filter stage, and according to the filtering R_3 and C_3 flows through R_2, C_2, and C_1 (the combination of which will be called Z_{for}). Feedback action of the op amp is intended to keep the negative input fixed at the same voltage as the reference, so the negative input is a "virtual ground". If the virtual ground condition is achieved, it frees up the values of R_3 and C_3 in the sense that they are isolated from and do not interact with other poles. However, op amp bandwidth limits in the case of a single pole prior to the op amp can cause error in this assumption. The inverting input is really only a virtual ground for signals whose frequency content is restricted to be within the bandwidth of the op amp.

It is often recommended that this input pole be the highest of the 3 poles so that better noise filtering is pushed forward in the filter. However, there is sometimes reason based on noise performance and synthesizer and op amp limits to make the R_3C_3 pole the middle pole. For example, one good reason is to better filter digital pulses presented to the inverting op amp input, even though doing so will associate the highest pole with C_1 and result in smaller C_1.

Note that while the relatively low reference voltage within the limits of the synthesizer charge pump is maintained on the op amp inputs, no such limit applies to the op amp output. It will "pump up" via current flowing through Z_{for} to assume whatever voltage is needed to maintain lock. Low noise op amps with supplies up to 36V are commonly available. Furthermore, unlike the non-inverting form with gain, this inverting form can with proper design assume these higher tune voltages with very little noise gain applied to the rms sum of the reference voltage noise and op amp noise.

The analysis to develop a design procedure begins similarly to the passive cases above. The 4th order filter case will be shown here. For transfer impedance Z(f) we find:

Equation 68: $$\boldsymbol{Z(s) = \frac{V_{out}}{I_{pd}} = \frac{1+sT_2}{s\,A_0(1+sT_1)(1+sT_3)(1+sT_4)}}$$

An importance difference from the passive case is that we shall set the output filter pole of T_4 to be the lowest frequency pole. The other poles shall then be referenced to this pole in terms of spacing.

We also find, due to the isolating effects of the op amp, that A_0 is not the total sum of capacitance, but instead:

Equation 69: $$\boldsymbol{A_0 = C_1 + C_2}$$

The open loop gain as a function of jω is:

Equation 70: $$\mathbf{GH(j\omega)} = \frac{K_d \mathrm{K_o}}{-N} \frac{1+j\omega T_2}{\omega^2 A_0 (1+j\omega T_1)(1+j\omega T_3)(1+j\omega T_4)}$$

Using the magnitude function of the open loop transfer function (1 at loop BW):

Equation 71: $$A_0 = \frac{K_d \mathrm{K_o}}{N\omega_L^2} \frac{\sqrt{1+\omega_L^2 {T_2}^2}}{\sqrt{(1+\omega_L^2 {T_1}^2)(1+\omega_L^2 {T_3}^2)(1+\omega_L^2 {T_4}^2)}}$$

Again, we are going to use T_4 here as the lowest frequency pole. We get T_4 and T_2 from the phase margin and derivative of phase margin relationships. We get T_1 and T_3 from the pole ratios selected. Most commonly these pole ratios are selected sequentially from the lowest pole to the next highest, and from that pole to the very highest. For example, if $f_3 > f_1$, then $T_3 < T_1$ and it would be standard practice to use pole ratio $T_{31} < 1$ with $T_3 = T_{31}T_1$. But, in this case there are times it is advantageous to use $f_3 > f_1$ and others where f3 < f1. So, in order to maintain one set of equations, we shall use the more general case where both higher frequency poles are references to the lowest pole f4. Typically, these poles are spaced from each other by approximately factors of two.

To evaluate A_0 we need T_4 and T_2, and we then use the selected pole ratios to get T_1 and T_3. The exact equations are:

Equation 72: $$\phi_m = \tan^{-1}(\omega_L T_2) - \tan^{-1}(\omega_L T_4) - \tan^{-1}(\omega_L T_{14} T_4) - \tan^{-1}(\omega_L T_{34} T_4)$$

Applying the first derivative test with general frequency ω, and setting the derivative to zero at $\omega = \omega_L$:

Equation 73: $$\frac{T_2}{1+\omega_L^2 T_2^2} - \frac{T_1}{1+\omega_L^2 T_4^2} - \frac{T_{14} T_4}{1+\omega_L^2 T_{14}^2 T_4^2} - \frac{T_{34} T_4}{1+\omega_L^2 T_{34}^2 T_4^2} = 0$$

Now these two may be solved numerically for T_2 and T_4, leading then to T_1 and T_3 via the selected pole ratios. The below approximations may be used as starting points for the numerical solutions, or used as is.

Equation 74: $$\phi_m = \tan^{-1}\left(\frac{\gamma}{\omega_L T_4 (1+T_{14}+T_{34})}\right) - \tan^{-1}(\omega_L T_4) - \tan^{-1}(\omega_L T_{14} T_4) \tan^{-1}(\omega_L T_{34} T_4)$$

We may use $\gamma = 1$, or alter it from 1 based on the optimization criteria in Banerjee 5th ed, chapter 36. The only variable remaining is T_4, which may be solved numerically, or approximately from:

Equation 75: $$T_4 \cong \frac{\frac{1}{\cos\phi_m} - \tan\phi_m}{\omega_L(1+T_{14}+T_{34})}$$

If the full approximate form is used, then:

Equation 76: $$T_2 \cong \frac{\gamma}{\omega_L^2\,(T_1+T_3+T_4)}$$

In either exact or either of the approximate cases:

Equation 77: $$T_1 = T_{14}\,T_4$$

Equation 78: $$T_3 = T_{34}\,T_4$$

We now have all the time constants needed to find $A_0 = C_1 + C_2$ from the magnitude equation. We may then find all the part values in Z_{for} from:

Equation 79: $$C_1 = \frac{T_1 A_0}{T_2}$$

Equation 80: $$C_2 = A_0 - C_1$$

Equation 81: $$R_2 = \frac{T_2}{C_2}$$

Now we come to selecting the values for R_3, C_3, R_4, and C_4. These seem easy to do because of the isolation provided by the op amp and having the time constants, but there are some subtle complexities at work here, and a need to deal with op amp limits.

On the input side of the op amp it might seem that smaller R_3 would help with noise, but actually the opposite is true. The thermal noise of R_3 is going up with its square root, whereas its noise gain is going down directly with R_3, so that the noise contribution of R_3 at the output of the op amp is going down with its square root (equations deferred to article 2) as R_3 increases. So, we are led to wanting R_3 as large as possible for noise reasons. This is another reason for having f_3 be the middle pole (the middle pole has larger RC) instead of the highest pole, along with the earlier stated reason of reducing the high frequency content the op amp is exposed to.

But, there is another trade-off here, which is that for larger R_3 is it possible for the average charge pump current in frequency acquisition mode to force the voltage on C_3 against the charge pump rail. This would shut down the charge pump current and lengthen the frequency acquisition time. This is particularly true when driving wide tune

range VCO's (some as wide as an octave are available) that must move through a large frequency range.

It's not a hard analysis to get to some useful approximate design equations to trade noise against the potential for acquisition slowing (if these are published elsewhere, the author is not aware of it and apologizes for lack of referencing). This will help designers avoid the situation of running into slow acquisition processes that are assumed to be simply the nature of the frequency lock settling mode, but may actually be more limited by the combination of charge pump and op amp limits.

We begin the analysis on the input side of the op amp. Banerjee gives (Ref. 13, 5th ed, p.38) the duty cycle of the phase-frequency detector in frequency lock mode as a function of the ratio of f_{ref} and f_{out}/N as:

Equation 82: $$D_c = 1 - \frac{f_{lower}}{f_{upper}}$$

In the above f_{lower} is the smaller of f_{ref} and f_{out}/N. Since most VCO's do not steer far in a fractional sense from their center frequency, such that f_{ref} and f_{out}/N are relatively close, the duty cycle would seldom range above 10% (octave type VCO's being the exception). D_c will be largest at the beginning of the channel change or acquisition process, approaching zero as the VCO converges towards the desired frequency.

Let us define ΔV_{mC3} as the max filtered voltage change from V_{ref} that we wish to be imposed on C_3 during a frequency lock acquisition event. For example, if V_{ref} = 2.4V (which we might use to stay in the common mode input range of a low noise op amp), with a charge pump supply of 3.3V, then we would probably not want the filtered voltage on C_3 to rise above about 2.9V in order to not choke off the positive (source) charge pump. In that case, ΔV_{mC3} would be 0.5V. We may thus write a relationship for R_{3max} as:

Equation 83: $$R_{3max} = \frac{\Delta V_{mC3}}{D_c I_{pd}}$$

The designer may use R_3 values up to R_{3max} with the R_3C_3 pole as either the highest frequency pole or the middle pole. We are trying to avoid R_3 being too small because of noise gain in the op amp, where the noise gain relative to reference and op amp noise is:

Equation 84: $$NoiseGain1(s) = 1 + \frac{Z_{for}(s)}{Z_{back}(s)}$$

For noise gain purposes, Z_{back} is the series combination of R_3 and C_3 to ground. The charge pump does not materially affect this impedance looking back from the op amp negative input because the pump is in a very high impedance off state most of the time, and even when on it is a high impedance current source. The fact that the largest D_c is usually in the range of 0.05 to 0.1 helps with allowing a large enough R_3 that Z_{back} is >> than Z_{for}. However, we have to be wary of D_c in the case of wide tuning VCO's. In that

case, we can program a large frequency change in smaller steps to avoid high D_c that can limit the size of R_3.

There are a set of slew rate requirements we need to consider, primarily in frequency lock acquisition mode for acquisition speed, and in phase lock mode for noise control. There are two cases of each. Banerjee offers experimental evidence (Ref. 13, 5th ed., pp.371-372) that if the op amp is not fast enough in the phase lock mode there will be worsening of 1/f phase noise inside the loop bandwidth. The "slow slew" active loop filter recommended here should reduce this effect. If the standard form is insufficient, then splitting the input pole into two poles is likely to help.

The worst case (highest) requirement on slew rate is during the frequency locking mode (when the phase detector is acting as a frequency detector) and where we may consider the loop to be acting at frequencies above the zero frequency f_2 where Z_{for} is dominated by R_2. This will be the case for moderate frequency jumps where "cycle slipping" of the phase detector is of brief duration. At the beginning of such a frequency acquisition process the phase detector duty cycle D_c is at a maximum and the phase/frequency detector current is charging C_3 with a ramp that must be followed on the op amp output. As this ramp progresses, the current through R_3 becomes significant and the ramp bends over (R_3 has been selected as above to force this to happen), but the worst case we must account for is the beginning phase of the ramp up on C_3. So, this is fundamentally a situation where C_3's average voltage change is according to the average charge pump current, leading to a voltage ramp that is multiplied by the effective gain of the op amp circuit. To keep the op amp locked with $V_{neg} = V_{plus}$, the op amp must slew according to the charge up and gain. This gives:

Equation 85: $$ReqSlewRateFLL(R_2\ limited) \cong \frac{D_{cmax} I_{pd}}{C_3} \frac{R_2}{R_3}$$

This slew requirement is reduced since for noise reasons we select $R_2/R_3 < 1$, but it can still be a fairly high slew rate requirement for low noise op amps and wide loop bandwidths with resulting small C_3. If it cannot be met with the desired op amp, the result will be a slowing of the frequency lock process.

There is another slew rate case for the frequency lock mode, which is the wide frequency acquisition mode that slowly occurs over a time that is much longer than T_2. In this time interval C_2 dominates Z_{for}, and the voltage on C_3 ramps up and reaches its maximum of ΔV_{mC3} fairly early in the process. The remaining acquisition time is dominated by the current $D_c I_{pd}$ flowing through R_3 and then through C_2 (C_3 being assumed negligible). This leads directly to:

Equation 86: $$ReqSlewRateFLL(C_2\ lim) \cong \frac{D_{cmax} I_{pd}}{C_2} = \frac{\Delta V_{mC3}}{R_3 C_2}$$

Since $C_2 > C_3$, and $R_2/R_3 < 1$, this limit is usually much smaller than the R_2 limit of FLL mode slew rate. The only way it can be larger is if D_{cmax} in this mode is so much larger

that it makes up for those differences. Furthermore, the loop that starts with wide frequency error and large D_c much eventually close its frequency error to the point that it enters the normally faster mode where the slew rate is dominated by R_2. So, while this slew rate case is worth calculating, it will normally be the case that the R_2 limited slew rate is larger and must be used for op amp selection.

The phase lock mode establishes a different slew rate requirement, one where ideally we want the op amp output to follow the voltage change imposed on C_3 during a charge pump on time interval. Normally op amp bandwidth will not allow this to happen, but we may still select poles and parts so that slew rate is not a limit. Since we are normally dealing with high frequency pulses, this desired behavior will usually be eased by the presence of C_1, which reduces the forward impedance around the op amp in the frequency band of the pulses, and thus the closed loop gain of the op amp at high frequencies. Let us consider R_2 as effectively open at these frequencies (above f_1), such that Z_{for} is dominated by C_1. We have a situation where the charge pump current ramps up the voltage on C_3 and the current in R_3 similarly ramps according to $I_{R3} = V_{C3}/R_3$ (the drain through R_3 being too small to affect the voltage on C_3 over the narrow pulse width time). Then over the interval of time from 0 to pulse width T_{pd}:

Equation 87: $$I_{R3} \cong \frac{I_{pd}\, t}{R_3 C_3} = I_{C1}$$

The voltage change on C_1 over the pulse time is the same as the voltage change on the op amp output. So:

Equation 88: $$V_{opamp} = \frac{1}{C_1}\int_0^t I\, dt \cong \frac{1}{C_1}\int_0^t \frac{I_{pd}\, t}{R_3 C_3} dt = \frac{I_{pd}\, t^2}{2 C_1 R_3 C_3}$$

Now taking the derivative of this with respect to time, which establishes the desired slew rate:

Equation 89: $$\frac{dV_{opamp}}{dt} \cong \frac{I_{pd}\, t}{C_1 R_3 C_3}$$

The desired slew rate of the op amp is changing over the pulse, but it reaches its maximum at the pulse width T_{pd}:

Equation 90: $$ReqSlewRatePLL(with\ C_1) \cong \frac{I_{pd}\, T_{pd}}{C_1 R_3 C_3}$$

This slew rate will normally be at least an order of magnitude less than that predicted in the frequency lock mode. This reduction in the slew rate requirement for the PLL mode is one of the benefits of including C_1 in the loop filter circuit. If the FLL mode slew rate is not met, then even if the frequency acquisition is slowed, the op amp may still meet

this requirement and perform well in PLL mode. Another benefit is that C_1 will reduce the op amp ringing transient response to the pulses from the charge pump. Even when the ringing in the op amp output is only in the range of a few hundred microvolts (typical if C_1 is not used), and then filtered by the output RC filter, it can still induce very visible spurs at frequencies around the op amp bandwidth where this slight ringing occurs. This will be discussed further in article 2 on noise.

For completeness the PLL slew rate case where C_1 is not used is given next. During the pulse time the voltage on C_3 is ramping at I_{pd} t / C_3, and the slew rate must support this being gained by R_2/R_3:

Equation 91: $$\boldsymbol{ReqSlewRatePLL(no\ C_1) \cong \frac{I_{pd}}{C_3}\frac{R_2}{R_3}}$$

This is a much steeper slew rate requirement. Taking the ratio of these two PLL mode slew rates:

Equation 92: $$\frac{\mathbf{SlewRatePLL(no\ C_1)}}{\mathbf{SlewRatePLL(with\ C_1)}} \cong \frac{\mathbf{R_2C_1}}{\mathbf{T_{pd}}}$$

Normally R_2C_1 is much greater than the pulse width time on the order of 1E-9. In practice the required slew rate increase without C_1 can exceed one thousand.

The alert reader will notice in the above slew rate presentation that op amp bandwidth was not mentioned. Of course, slew rate is a partial surrogate for bandwidth, but the story told above is still incomplete. Few op amps are going to actually be able to follow the voltage changes on C_3 during a single pulse time—even when judicious pole and part selection and their slew rate allows them to, their bandwidth limits often will not. Instead the change in op amp output (despite being damped by C_1 and by opposite pulses partially canceling previous ones) occur over a period of time that is approximately $1/G_{bw}$, where G_{bw} is the gain-bandwidth product of the op amp. With modern synthesizers using very high phase detector frequencies, this will typically range from about 1 to 10 phase detector periods. As pointed out by Banerjee, experimental evidence (Ref. 13, 5th ed., pp.371-372) indicates that the op amp not being fast enough can cause a several dB rise in the 1/f noise of the PLL due to pulse widening allowing through more charge pump 1/f noise. The term "fast enough" encompasses both slew and bandwidth.

The situation with op amp bandwidth possibly widening charge pump pulses is one that calls for greater investigation. However, a logical step should a noticeable increase in 1/f noise be a concern with the 4th order active loop filter is to add another high frequency pole on the input side of the op amp. By this it is meant to break the R_3C_3 pole into two poles, with a 5th order filter and a 6th order loop being the result. The problem with the standard single pole on the op amp input is that the charge pump pulse is converted to a narrow ramp of voltage, which despite limited amplitude change is still a fast rise time on the order of 1ns. An additional pole can covert this ramp to a much slower nearly

exponential shape. If this pole does not exceed 0.1 to 0.2 of the op amp GBW it can place the majority of frequency content inside the bandwidth of the op amp. It should also further suppress spurs from the ringing response of the op amp to charge pump pulses (the op amp is being hit with smoothed inputs and not a sharper edged ramp).

A brief summary of op amp bandwidth is appropriate here. A common rule of thumb is for op amp GBW to be at least 10X PLL loop BW, as is typical of other op amp circuits. However, the author contends that in the case of the ultra-low noise synthesizer, this may be inadequate bandwidth due to the sampled nature of the modern PLL with its very narrow charge pump pulses. Instead, we should consider op amp bandwidth in the context of the op amp successfully responding to the bandwidth of the filtered digital signals that reach its input. Even the "slow slew" filter recommended here often suffers from failure to exactly follow the input signal when there is only a single RC stage preceding the op amp. If it is desired to achieve the best 1/f noise and minimum spurs by avoiding pulse widening, the author recommends an additional input filter stage to slow the signals further to be within the bandwidth of the op amp selected. The basic strategy may be described as selecting a rather fast low noise op amp, and then "cocooning" it within adequate filtering, such that the op amp is not expected to do more than its specifications dictate it can do. Getting adequate filtering to protect the op amp may require reducing the PLL loop bandwidth below optimum for minimum jitter (to be covered in article 2), so there can be a trade-off here between better 1/f noise, and better noise around the loop bandwidth.

Next, we consider the op amp limits on C_4. The possible issue here is normally the maximum output current of the op amp. We are used to seeing DC load limits on op amps in the range of 500 ohms to 5k, and relatively low values of capacitance that can be directly driven without the op amp becoming unstable. However, many op amps can drive loads of surprisingly small resistance isolating a large capacitor. We find 10 ohms and even less is often not a problem to isolate capacitance of 1µF or more. But, when we impose a large frequency change on the PLL, that large capacitance does take large current to change voltage quickly. The short term (before thermal limits take effect) upper current limit on op amps is usually in the range of 10mA to 100mA. If we try to force an op amp in the FLL mode to exceed this, we will hit a maximum ramp rate on C_4, and the slow frequency lock mode acquisition process will be slowed still further.

Fundamentally, we desire the op amp max current I_{opmax} to be able to charge C_4 at the same rate that D_c*I_{pd} charges C_2. Using I*t = C*V, a few lines will show:

Equation 93: $$C_{4max} = \frac{I_{opmax} C_2}{D_c I_{pd}}$$

This maximum is often more than we would like to use for reasons of size and cost, and in some cases it may lead to unreasonably small values of R_4 that the op amp cannot drive. In that case we usually select a value of R_4 the op amp can drive whose thermal noise is still considerably less than the noise of the op amp, and then find $C_4 = T_4/R_4$. A possible consideration that could set a higher resistance on R_4 is op amp thermal limits in

the case of many wide frequency changes in a short period of time, such as a frequency hopping spread spectrum system, that repeatedly charge and discharge C_4 with large op amp currents.

Summary:

This first article out of four has introduced the subject of modern synthesizer design techniques to set the stage for the next three. Moving forward, we will find ourselves witnessing a battle between synthesizer IC makers who provide on-die VCO's and the providers of classic discrete VCO's. The discrete VCO providers have honed their art over a period of decades to provide very low noise VCO's for use in the bands that demand that kind of performance. Their out of loop bandwidth noise still sets the standard, sometimes by over 20dB, and is valuable for applications that demand that. But, the chip makers have mounted an asymmetric attack to offer a complete solution on one IC. They have done some astonishing work to put surprisingly good VCO's on the die, and followed that up with architectural steps that suppress noise in band to a greater degree than is possible with current lower frequency discrete VCO's. This is supported by steadily increasing availability and falling prices of high speed, high accuracy, and low noise crystal reference oscillators, with 100MHz becoming a recent standard that the latest chips can take full advantage of.

To maintain their noise advantage at all offset frequencies, discrete VCO manufacturers will need to provide higher VCO frequencies with similar normalized phase noise performance as their better low frequency application band VCO's. This would allow them to take advantage of the latest synthesizer innovations based on high VCO frequency to match or beat the in-band noise performance of the integrated competition. The high frequency VCO output is then divided down to the application band, picking up 6dB of phase noise improvement for every divide by two, just as in done for the integrated VCO's.

Article 2 will delve into these noise issues in greater depth. Article 3 will review the components and tools now available to the designer, with particular emphasis on the noise performance of the parts. Article 4 will then put all that information into example form for several different applications that demand the finest noise performance.

Article 1 References:

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Reg. 10: “Microwave and Wireless Synthesizers: Theory and Design”, Ulrich L. Rohde, John Wiley and Sons, 1997. This book is an update to the Rohde text just above.

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https://badw.de/fileadmin/members/R/3685/6_4_18_UNI_BW_June18-safe.pdf
This reference is particularly valuable for its combination of methods from basic to advanced, and resulting final limits.

Ref. 12: “An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump PLL’s”, National Semiconductor Application Note 1001, 1996, by Bill Keese. Though this reference was not the first to analytically present higher order loop filters, it became widely available via the early internet and had a strong influence.

Ref. 13: “PLL Performance, Simulation, and Design”, Dean Banerjee, first edition 1998 and 2001. The focus of this outstanding book is modern design focusing on synthesizers with high order loops and noise prediction using the normalized noise floor of the particular synthesizer chip to take into account divider and charge pump noise. It is currently in its 5th edition, published 2017, covering sigma delta synthesizers and their spur control methods in high detail. Author Dean Banerjee is an electrical engineer and applied mathematician who was deeply involved in the National Semiconductor effort to build a powerhouse synthesizer IC business (now owned by Texas Instruments), and this groundbreaking book reflects both his detailed insider knowledge and his ability to distill

practical design methods with tractable mathematics from the complexity of low noise synthesizer design. The 5th edition of 2017 may be freely downloaded in pdf form at: http://www.ti.com/tool/pll_book.

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Ref. 17: "Advanced Frequency Synthesis by Phase Lock", William Egan, John Wiley and Sons and the IEEE, 2011. This advanced reference assumes basic knowledge as presented in "Frequency Synthesis by Phase Lock" and similar texts so that it may focus on modern sigma delta synthesizer design methods.

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